AN3027
Application note

How to design a transition-mode PFC pre-regulator with the L6563S and L6563H

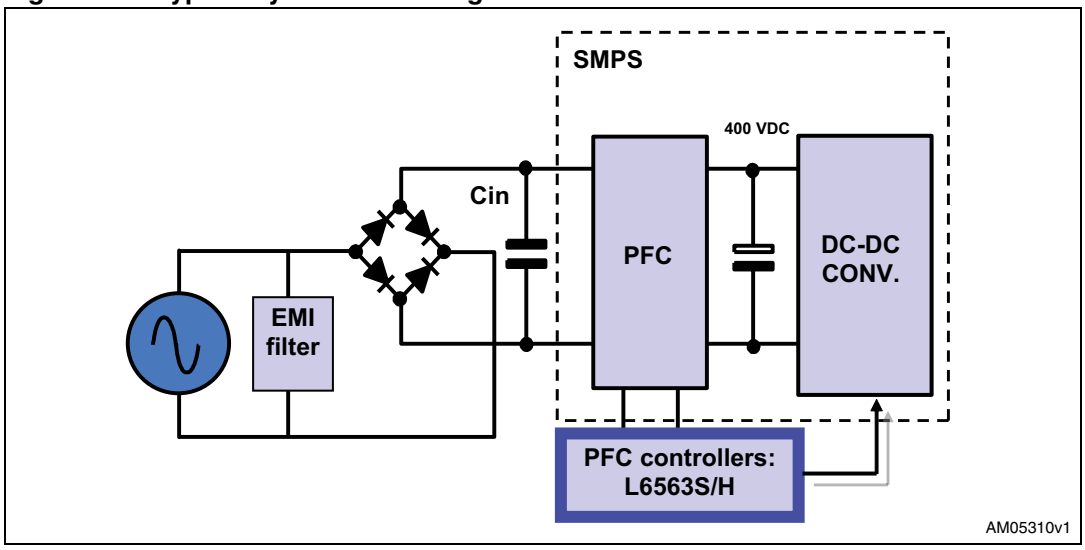
Introduction

The transition-mode (TM) technique is widely used for power factor correction in low and middle power applications such as lamp ballasts, high-end adapters, flatscreen TVs and monitors, PC power supplies and all SMPS having to meet regulations in harmonics reduction. The L6563S and L6563H are the latest devices from STMicroelectronics for these applications that may require a low-cost power factor correction.

The L6563S is a current-mode PFC controller operating in transition mode (TM). Packaged in the same SO14 pinout as its predecessor L6563, it offers improved performance and additional functions. The L6563H is the SO16 pinout version, embedding the same features as the L6563S with the addition of a high-voltage startup power source.

These functions make the L6563H especially suitable for applications that need to be compliant with energy-saving regulations and where the PFC pre-regulator works as the master stage without an auxiliary SMPS.

Figure 1. Typical system block diagram



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1 Introduction to power factor correction

The front-end stage of conventional offline converters, typically consisting of a full-wave rectifier bridge with a capacitor filter, has an unregulated DC bus from the AC mains. The filter capacitor must be large enough to have a relatively low ripple superimposed on the DC level. This means that the instantaneous line voltage is below the voltage on the capacitor most of the time, thus the rectifiers conduct only for a small portion of each line half-cycle.

The current drawn from the mains is a series of narrow pulses whose amplitude is 5-10 times higher than the resulting DC value. Many drawbacks result, such as a much higher peak and RMS current down from the line, distortion of the AC line voltage, overcurrents in the neutral line of the three-phase systems and, consequently, a poor utilization of the power system's energy capability. This can be measured in terms of either total harmonic distortion (THD), as norms provide for, or power factor (PF), intended as the ratio between the real power (the one transferred to the output) and the apparent power (RMS line voltage multiplied by the RMS line current) drawn from the mains, which is more immediate. A traditional input stage with capacitive filter has a low PF (0.5-0.7) and a high THD (>100%).

By using switching techniques, a power factor corrector (PFC) preregulator, located between the rectifier bridge and the filter capacitor, allows drawing a quasi-sinusoidal current from the mains, in phase with the line voltage. The PF becomes very close to 1 (more than 0.99 is possible) and the previously mentioned drawbacks are eliminated. Theoretically, any switching topology can be used to achieve a high PF but, in practice, the boost topology has become the most popular thanks to the advantages it offers:

- Primarily because the circuit requires the fewest external parts (low-cost solution)
- The boost inductor located between the bridge and the switch causes the input di/dt to be low, thus minimizing the noise generated at the input and, therefore, the requirements on the input EMI filter
- The switch is source-grounded, therefore easy to drive

However, boost topology requires the DC output voltage to be higher than the maximum expected line peak voltage (400 VDC is a typical value for 230 V or wide-range mains applications). In addition, there is no insulation between the input and output, thus any line voltage surge is passed on to the output. Two methods of controlling a PFC pre-regulator are currently widely used: the fixed-frequency, average current mode PWM (FF PWM) and the transition mode (TM) PWM (fixed on-time, variable frequency). The first method needs complex control that requires a sophisticated controller IC (ST's L4981, with the variant of the frequency modulation offered by the L4981) and a considerable component count. The second one requires a simpler control (implemented by ST's L6563S), much fewer external parts and is therefore much more economical. With the first method the boost inductor works in continuous conduction mode, while TM makes the inductor work on the boundary between continuous and discontinuous mode, by definition. For a given throughput power, TM operation involves higher peak currents. This, also consistent with cost considerations, implies its use in a lower power range (typically up to 250 W), while the former is recommended for higher power levels. To conclude, FF PWM is not the only alternative when CCM operation is desired. FF PWM modulates both switch-on and switch-off times (their sum is constant by definition), and a given converter operates in either CCM or DCM depending on the input voltage and the load conditions. Exactly the same result can be achieved if the on-time only is modulated and the off-time is kept constant, in which case, however, the switching frequency is no longer fixed. This is referred to as “fixed-off-time” (FOT) control. Peak-current-mode control can still be used. In this application note transition mode is studied in depth.

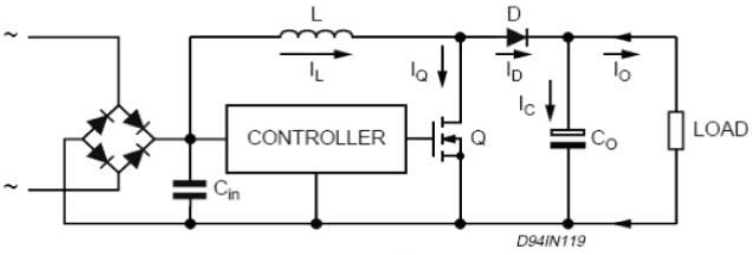
2 TM PFC operation (boost topology)

The operation of the PFC transition mode controlled boost converter can be summarized in the following description.

The AC mains voltage is rectified by a bridge and the rectified voltage is delivered to the boost converter. This, using a switching technique, boosts the rectified input voltage to a regulated DC output voltage (Vo).

The boost converter consists of a boost inductor (L), a controlled power switch (Q), a catch diode (D), an output capacitor (Co) and, obviously, a control circuit (see figure below). The goal is to shape the input current in a sinusoidal fashion, in phase with the input sinusoidal voltage. To do this, the L6563S uses the transition mode technique.

Figure 2. Boost converter circuit



The error amplifier compares a partition of the output voltage of the boost converter with an internal reference, generating an error signal proportional to the difference between them. If the bandwidth of the error amplifier is narrow enough (below 20 Hz), the error signal is a DC value over a given half-cycle.

The error signal is fed into the multiplier block and multiplied by a partition of the rectified mains voltage. The result is a rectified sinusoid whose peak amplitude depends on the mains peak voltage and the value of the error signal.

The output of the multiplier is in turn fed into the (+) input of the current comparator, thus it represents a sinusoidal reference for PWM. In fact, when the voltage on the current sense pin (instantaneous inductor current multiplied by the sense resistor) equals the value on the (+) of the current comparator, the conduction of the MOSFET is terminated. As a consequence, the peak inductor current is enveloped by a rectified sinusoid. As demonstrated in *Section 3.3.4*, TM control causes a constant on-time operation over each line half-cycle.

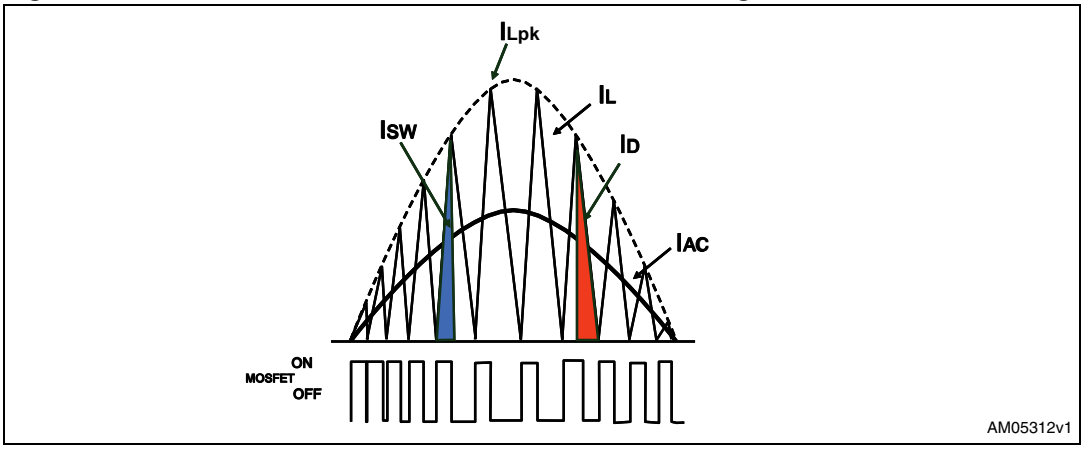
After the MOSFET has been turned off, the boost inductor discharges its energy into the load until its current goes to zero. The boost inductor has now run out of energy, the drain node is floating and the inductor resonates with the total capacitance of the drain. The drain voltage drops rapidly below the instantaneous line voltage and the signal on ZCD drives the MOSFET on again and another conversion cycle starts.

This low voltage across the MOSFET at turn-on reduces both the switching losses and the total drain capacitance energy that is dissipated inside the MOSFET.

The resulting inductor current and the timing intervals of the MOSFET are shown in *Figure 3*, where it is also shown that, by geometric relationships, the average input current

(the one which is drawn from the mains) is just one-half of the peak inductor current waveform.

Figure 3. Inductor current waveform and MOSFET timing



The system operates not exactly on, but very close to, the boundary between continuous and discontinuous current mode and that is why this system is called a transition mode PFC. Besides the simplicity and the few external parts required, this system minimizes the inductor size due to the low inductance value needed. On the other hand, the high current ripple on the inductor involves high RMS current and high noise on the rectified main bus, which needs a heavier EMI filter to be rejected. These drawbacks limit the use of the TM PFC to lower power range applications.

3 Designing a TM PFC

The following section describes a design flowchart of a 100 W transition mode PFC, using the L6563S. The same design procedure and formulas proposed can also be applied for dimensioning a similar 100 W transition mode PFC, using the L6563H.

3.1 Input specifications

This section details the specifications of the operating conditions of the circuit that are needed for the calculations given in *Section 3.2*. In this example an L6563S, wide input range mains PFC circuit has been considered. Some design criteria are also given.

- Mains voltage range (Vac rms): $VAC_{min} = 90Vac \quad VAC_{max} = 265Vac$ (1)

- Minimum mains frequency $f_{MAINS} = 47\ Hz$ (2)

- Rated output power (W): $P_{out} = 100\ W$ (3)

Because the PFC is a boost topology, the regulated output voltage depends mainly on the maximum AC input voltage. In fact, for correct operation the output voltage must be always higher than the input and thus, because V_{in} max is 265·1.414 = 374.7 Vpk, the output has been set at 400 Vdc as typical value. If the input voltage is higher, as is typical in ballast applications, the output voltage must be set higher accordingly. As a rule of thumb, the output voltage must be set 6/7% higher than the maximum input voltage peak.

- Regulated DC output voltage (Vdc): $V_{out} = 400\ V$ (4)

The target efficiency and PF are set here at minimum input voltage and maximum load. They are used for the calculations of the operating conditions of the PFC in *Section 3.2*. Of course at high input voltage, the efficiency is higher.

- Expected efficiency (%): $\eta = 94\%$ (5)

- Expected power factor: $PF = 0.99$ (6)

Because of the narrow loop voltage bandwidth, the PFC output can face overvoltages at startup or in the case of load transients. To prevent excessive output voltage that can overstress the output components and the load, in the L6563S a pin of the device (PFC_OK, pin #7) has been dedicated to monitor the output voltage with a separate resistor divider, selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset

value (V_{OVP}), usually larger than the maximum V_{out} that can be expected, also including worst-case load/line transients.

- Maximum output voltage (Vdc): $V_{OVP} = 430$ V (7)

The mains frequency generates a $2f_{MAINS}$ voltage ripple on the output voltage at full load. The ripple amplitude determines the current flowing into the output capacitor and the ESR. Additionally, a request for a certain hold-up capability can be sent to the PFC if mains dips occur in which case the output capacitor also must be dimensioned, taking into account the required minimum voltage value ($V_{out\,min}$) after the hold-up time (t_{Hold}) has elapsed.

- Maximum output low-frequency ripple: $\Delta V_{out} = 20$ V (8)

- Minimum output voltage after line drop (Vdc): $V_{out\,min} = 300$ V (9)

- Hold-up capability (ms): $t_{Hold} = 10$ ms (10)

The PFC minimum switching frequency is the one of the main parameters used to dimension the boost inductor. Here we consider the switching frequency at low mains on the top of the sinusoid and at full load conditions. As a rule of thumb, it must be higher than the audio bandwidth in order to avoid audible noise and additionally it must not interfere with the L6563S minimum internal startup period, given in the datasheet. On the other hand, if the minimum frequency is set too high, the circuit shows excessive losses at a higher input voltage and probably skips switching cycles not only at light load. The typical minimum frequency range is 20 - 50 kHz for wide range operation.

- Minimum switching frequency (kHz): $f_{sw\,min} = 40$ kHz (11)

In order to properly select the power components of the PFC and dimension the heatsinks in case they are needed, the maximum operating ambient temperature around the PFC circuitry must be known. Please note that this is not the maximum external operating temperature of the entire system, but it is the local temperature at which the PFC components are working.

- Maximum ambient temperature (°C): $T_{ambx} = 50°C$ (12)

3.2 Operating conditions

The first step is to define the main parameters of the circuit, using the specifications given in *Section 3.1*.

- Rated DC output current:

Equation 1

$$I_{out} = \frac{P_{out}}{V_{out}} \qquad I_{out} = \frac{100\ W}{400\ V} = 0.25\ A$$

- Maximum input power:

Equation 2

$$P_{in} = \frac{P_{out}}{\eta} \qquad P_{in} = \frac{100\ W}{94} \cdot 100 = 106.38\ W$$

- RMS input current:

Equation 3

$$I_{in} = \frac{P_{in}}{VAC_{min} \cdot PF} \qquad I_{in} = \frac{106.38\ W}{90Vac \cdot 0.99} = 1.19\ A$$

- Peak inductor current:

Equation 4

$$IL_{pk} = 2 \cdot \sqrt{2} \cdot I_{in} \qquad IL_{pk} = 2 \cdot \sqrt{2} \cdot 1.19\ A = 3.38\ A$$

As shown in *Figure 3*, the inductor current is a triangle shape at the switching frequency, and the peak of the triangle is twice its average value. The average value of the inductor current is exactly the peak of the input sine wave current, and therefore it can be easily calculated as its RMS value can be obtained from *Equation 3*. In order to provide a complete inductor specification for the inductor manufacturer, we must also provide the RMS and the AC current that can be calculated using *Equation 5* and *Equation 6*.

- RMS inductor current:

Equation 5

$$IL_{rms} = \frac{2}{\sqrt{3}} \cdot I_{in} \qquad IL_{rms} = \frac{2}{\sqrt{3}} \cdot 1.19\ A = 1.38\ A$$

- AC inductor current:

Equation 6

$$IL_{ac} = \sqrt{IL_{rms}^2 - I_{in}^2} \qquad IL_{ac} = \sqrt{(1.38)^2 - (1.19\ A)^2} = 0.69\ A$$

The current flowing in the inductor can be split in two parts, depending on the conduction instant. During the on-time, the current increases from zero up the peak value and circulates into the switch, while during the following off-time the current decreases from its peak down to zero and circulates into the diode. Therefore these two components have a current with a triangular wave, with the same peak value equal to that of the inductor. Thus, it is also possible to calculate the RMS current flowing into the switch and into the diode, needed to calculate the losses of these two elements.

- RMS switch current:

Equation 7

$$ISW_{rms} = IL_{pk} \cdot \sqrt{\frac{1}{6} - \frac{4 \cdot \sqrt{2}}{9\pi} \cdot \frac{VAC_{min}}{V_{out}}} \qquad ISW_{rms} = 3.38\ A \cdot \sqrt{\frac{1}{6} - \frac{4 \cdot \sqrt{2}}{9\pi} \cdot \frac{90Vac}{400\ V}} = 1.18\ A$$

- RMS diode current:

Equation 8

$$ID_{rms} = IL_{pk} \cdot \sqrt{\frac{4 \cdot \sqrt{2}}{9\pi} \cdot \frac{VAC_{min}}{V_{out}}} \qquad ID_{rms} = 3.38\ A \cdot \sqrt{\frac{4 \cdot \sqrt{2}}{9\pi} \cdot \frac{90Vac}{400\ V}} = 0.72\ A$$

3.3 Power section design

3.3.1 Bridge rectifier

The input rectifier bridge can use standard slow recovery, low-cost devices. Typically a 600 V device is selected in order to have good margin against mains surges. An NTC resistor limiting the current at turn-on is required to avoid excessive stress to the diode bridge.

The rectifier bridge power dissipation can be calculated using *Equation 9*, *Equation 10*, *Equation 11*. The threshold voltage and dynamic resistance of a single diode of the bridge can be found in the datasheet of the device.

Equation 9

$$\bar{I}_{inrms} = \frac{\sqrt{2} \cdot I_{in}}{2} = \frac{\sqrt{2} \cdot 1.19\ A}{2} = 0.84\ A$$

Equation 10

$$\bar{I}_{in_avg} = \frac{\sqrt{2} \cdot I_{in}}{\pi} = \frac{\sqrt{2} \cdot 1.19\ A}{\pi} = 0.54\ A$$

The power dissipated on the bridge GBU4J is:

Equation 11

$$P_{bridge} = 4 \cdot R_{diode} \cdot \bar{I}^2_{inrms} + 4 \cdot V_{th} \cdot \bar{I}_{in_avg}$$

$$P_{bridge} = 4 \cdot 0.04\ \Omega \cdot (0.84\ A)^2 + 4 \cdot 0.7\ V \cdot 0.54\ A = 1.62\ W$$

3.3.2 Input capacitor

The input high-frequency filter capacitor (C_{in}) has to attenuate the switching noise due to the high-frequency inductor current ripple (twice the average line current, *Figure 3*).

The worst conditions occur on the peak of the minimum rated input voltage. The maximum high-frequency voltage ripple across Cin is usually imposed between 5% and 20% of the minimum rated input voltage. This is expressed by a coefficient r (= 0.05, 0.2) as an input design parameter:

- Ripple voltage coefficient (%): $r = 0.15$ (13)

Equation 12

$$C_{in} = \frac{I_{in}}{2\pi \cdot f_{sw\,min} \cdot r \cdot VAC_{min}} \qquad C_{in} = \frac{1.19A}{2\pi \cdot 40\,kHz \cdot 0.15 \cdot 90Vac} = 0.359\,\mu F$$

In real conditions the input capacitance is designed to take the EMI filter into account and to have a tolerance on the component of about 5% -10% (typ. for polyester capacitors).

A commercial capacitor of C_{in} = 0.47 µF has been selected. Of course a bigger capacitor benefits the EMI but hurts the THD, especially at high mains. Therefore a compromise must be found between these two parameters. A good quality film capacitor for this component must be selected in order to have an effective filter.

3.3.3 Output capacitor

The selection of the output bulk capacitor (Co) depends on the DC output voltage *(4)*, the allowed maximum output voltage *(7)* and the converter output power *(3)*.

The 100/120 Hz (twice the mains frequency) voltage ripple (ΔVout = peak-to-peak ripple value) is a function of the capacitor impedance and the peak capacitor current:

Equation 13

$$\Delta V_{out} = 2 \cdot I_{out} \cdot \sqrt{\frac{1}{(2\,\pi \cdot 2f_l \cdot C_O)^2} + ESR^2}$$

With a low ESR capacitor the capacitive reactance is dominant, therefore:

Equation 14

$$C_O \geq \frac{I_{out}}{2\pi \cdot f_l \cdot \Delta V_{out}} = \frac{P_{out}}{2\pi \cdot f_{MAINS} \cdot V_{out} \cdot \Delta V_{out}} \qquad C_O \geq \frac{100W}{2\pi \cdot 47\,Hz \cdot 400\,V \cdot 20\,V} = 42.5\,\mu F$$

ΔVout is usually selected in the range of 1.5% of the output voltage. Although ESR usually does not affect the output ripple, it should be taken into account for calculating the power losses. The total RMS capacitor ripple current, including mains frequency and switching frequency components, is:

Equation 15

$$I_{Crms} = \sqrt{ID^2_{rms} - I^2_{out}} \qquad I_{Crms} = \sqrt{(0.72\,A)^2 - (0.25\,A)^2} = 0.67\,A$$

If the PFC stage has to guarantee a specified hold-up time, the selection criterion of the capacitance changes. Co has to deliver the output power for a certain time (t_{Hold}) with a specified maximum dropout voltage ($V_{out\ min}$) that is the minimum output voltage value (which takes load regulation and output ripple into account). It is also the minimum output operating voltage threshold before triggering the “power fail” detection and consequent stopping of the downstream system supplied by the PFC.

Equation 16

$$C_O = \frac{2 \cdot P_{out} \cdot t_{Hold}}{\left(V_{out} - \Delta V_{out}\right)^2 - V_{out\,min}^2} \qquad C_O = \frac{2 \cdot 100\ W \cdot 10\ ms}{(400\ V - 20\ V)^2 - (300\ V)^2} = 36.7\ \mu F$$

A 20% tolerance on the electrolytic capacitors has to be taken into account for the right dimensioning. As shown in *Equation 14*, for this application a capacitor C_O = 47 µF (450 V) has been selected in order to maintain a hold-up capability of 14 ms. The actual output voltage ripple with this capacitor is also calculated. In detail:

Equation 17

$$t_{hold} = \frac{C_O \cdot \left[\left(V_{out} - \Delta V_{out}\right)^2 - V_{out\,min}^2\right]}{2 \cdot P_{out}} \qquad t_{hold} = \frac{47\ \mu F \cdot \left[(400\ V - 20V)^2 - (300\ V)^2\right]}{2 \cdot 100\ W} = 14.78\ ms$$

As expected the ripple variation on the output is:

Equation 18

$$\Delta V_{out} = \frac{I_{out}}{2 \cdot \pi \cdot f_l \cdot C_O} \qquad \Delta V_{out} = \frac{0.25A}{2 \cdot \pi \cdot 47\ Hz \cdot 47\ \mu F} = 18.02\ V$$

3.3.4 Boost inductor

The boost inductor determines the operating frequency of the converter, thus it is usually calculated so that the minimum switching frequency is greater than the maximum frequency of the L6563S internal startup (150 µs typ.), to ensure correct TM operation. Assuming unity PF:

Equation 19

$$t_{on}(VAC, \vartheta) = \frac{L \cdot IL_{pk} \cdot \sin(\vartheta)}{\sqrt{2} \cdot VAC \cdot \sin(\vartheta)} = \frac{L \cdot IL_{pk}}{\sqrt{2} \cdot VAC}$$

Equation 19 demonstrates that the on-time doesn't depend on the mains phase angle, but it is constant over the entire mains cycle.

Equation 20

$$t_{off}(VAC, \vartheta) = \frac{L \cdot IL_{pk} \cdot \sin(\vartheta)}{V_{out} - \sqrt{2} \cdot VAC \cdot \sin(\vartheta)}$$

t_{on} and t_{off} represent respectively the on-time and the off-time of the power MOSFET. IL_{pk} is the maximum peak inductor current in a line cycle and θ is the instantaneous line phase of the interval [0,Π]). Note that the on-time is constant over a line cycle.

As previously stated, IL_{pk} is twice the line-frequency peak current *Equation 4*, which is related to the input power and the input mains voltage. Substituting this relationship in the expressions of t_{on} and t_{off}, after some algebra it is possible to find the instantaneous switching frequency along a line cycle:

Equation 21

$$f_{sw}(VAC,\theta) = \frac{1}{T_{on} + T_{off}} = \frac{1}{2 \cdot L \cdot P_{in}} \cdot \frac{VAC^2 \cdot \left(V_{out} - \sqrt{2} \cdot VAC \cdot \sin(\theta)\right)}{V_{out}}$$

The switching frequency is minimum at the top of the sinusoid ($\theta = \Pi/2$ ==> $\sin\theta = 1$), maximum at the zero crossings of the line voltage ($\theta = 1$ or Π ==> $\sin\theta = 0$), where $t_{off} = 0$.

The absolute minimum frequency f_{swmin} can occur at either the maximum VAC_{max} or the minimum mains voltage VAC_{min}, thus the inductor value is defined by the formula:

Equation 22

$$L(VAC) = \frac{VAC^2 \cdot (V_{out} - \sqrt{2} \cdot VAC)}{2 \cdot f_{sw\,min} \cdot P_{in} \cdot V_{out}}$$

After calculating the values of the inductor at low mains and at high mains $L(VAC_{max})$, $L(VAC_{min})$ *Equation 23*, the lowest value must be used. It becomes the maximum inductance value for the PFC dimensioning.

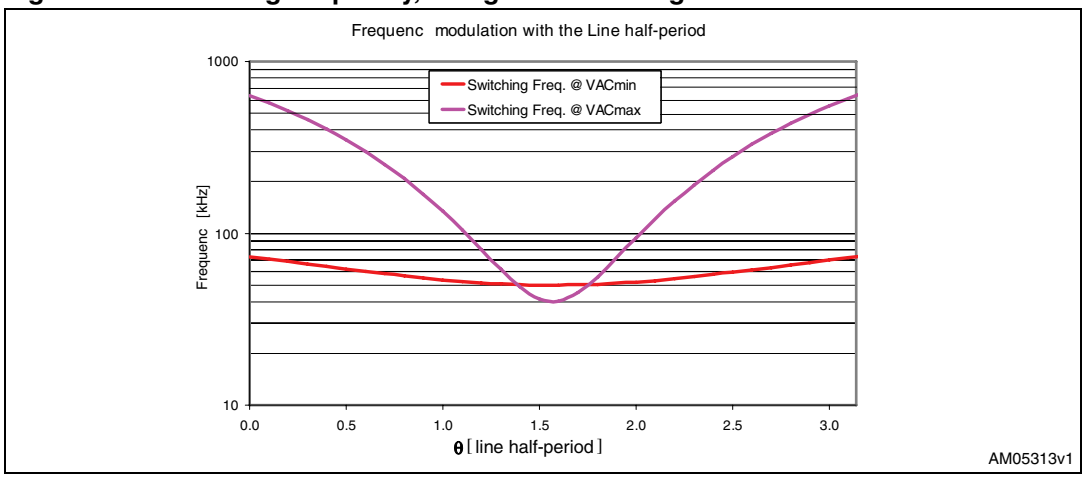
Equation 23

$$L(VAC_{min}) = \frac{(90Vac)^2 \cdot (400\ V - \sqrt{2} \cdot 90Vac)}{2 \cdot 40\ \ kHz \cdot 106.38\ W \cdot 400\ V} = 0.642\ mH$$

$$L(VAC_{max}) = \frac{(265Vac)^2 \cdot (400\ V - \sqrt{2} \cdot 265Vac)}{2 \cdot 40\ kHz \cdot 106.38\ W \cdot 400\ V} = 0.515\ mH$$

For this application a 0.52 mH boost inductance has been selected.

Figure 4. Switching frequency, fixing the line voltage



The figure above shows the switching frequency versus the θ angle calculated with *Equation 22*, a 0.52 mH boost inductance and fixing the line voltage at minimum and maximum

values. The minimum switching frequency can be recalculated for the selected inductance value, inverting the formula in *Equation 22* to the following:

Equation 24

$$f_{sw\,min}(VAC) = \frac{VAC^2 \cdot (V_{out} - \sqrt{2} \cdot VAC)}{2 \cdot L \cdot P_{in} \cdot V_{out}}$$

From the comparison of $f_{swmin}(VAC_{min})$ and $f_{swmin}(VAC_{max})$ with L = 0.52 mH as the actual, the calculated minimum switching frequency is 40.13 kHz, as expected.

The core size is determined, assuming a peak flux density Bx ≅ 0.25T (depending on the ferrite grade selected and relevant specific losses) and calculating the maximum current according to *Equation 45* as a function of the maximum clamping voltage of the current sense pin and sense resistor value.

DC and AC copper losses and ferrite losses must also be calculated to determine the maximum temperature rise of the inductor.

3.3.5 Power MOSFET selection and dissipation

The selection of the MOSFET concerns mainly its $R_{DS(on)}$, which depends on the output power *(3)*, since the breakdown voltage is fixed just by the output voltage *(4)*, plus the overvoltage admitted *(7)* and a safety margin (20%). Thus, a voltage rating of 500 V (1.2 · Vout = 480 V) is selected. Regarding its current rating as a rule of thumb, we can select a device having ~ 3 times the RMS switch current (see *Equation 7*), but the power dissipation calculation gives the final confirmation that the selected device is the right one for the circuit. The heatsink dimensions must also be considered. In this L6563S TM PFC application, an STF7NM50 MOSFET has been selected. The MOSFET' s power dissipation depends on conduction, switching and capacitive losses.

The conduction losses at maximum load and minimum input voltage are calculated by:

Equation 25

$$P_{cond}(VAC) = R_{DS(on)} \cdot (ISW_{rms}(VAC))^2$$

Because normally in datasheets the $R_{DS(on)}$ is given at ambient temperature (25 °C) to calculate correctly the conduction losses at 100°C (typical MOSFET junction operating temperature) a factor of 1.75 to 2 should be taken into account. The correct factor can be found in the device datasheet.

Now, the conduction losses referred to a 1 Ω $R_{DS(on)}$ at ambient temperature as a function of P_{in} and VAC can be calculated, combining *Equation 25* and *Equation 7*:

Equation 26

$$P'_{cond}(VAC) = 2 \cdot (ISW_{rms}(VAC))^2 = 2 \cdot \left(\frac{P_{in}}{\sqrt{2} \cdot VAC \cdot PF} \cdot \sqrt{2 - \frac{16}{3\pi} \cdot \frac{\sqrt{2} \cdot VAC}{V_{out}}} \right)^2$$

The switching losses in the MOSFET occur only at turn-off because of TM operation and can be basically expressed by:

Equation 27

$$P_{switch}(VAC) = V_{MOS} \cdot I_{MOS} \cdot t_{fall} \cdot f_{sw}(VAC)$$

Equation 27 represents the crossing between the MOSFET current that decreases linearly during the fall time and the voltage on the MOSFET drain that increases. In fact during the fall time, the current of the boost inductor flows into the parasitic capacitance of the MOSFET, charging it. For this reason, switching losses depend also on the total drain capacitance. Because the switching frequency depends on the input line voltage and the phase angle on the sinusoidal waveform, it can be demonstrated that from *Equation 27* the switching losses per 1 µs of current fall time and 1 nF of total drain capacitance can be written as:

Equation 28

$$P'_{switch}(VAC) = IL_{pk} \cdot V_{out} \cdot \frac{1}{\pi}\int_0^{\pi} (\sin\vartheta)^2 \cdot f_{sw}(VAC,\theta) \cdot d\vartheta$$

On the power MOSFET datasheet t_{fall} at turn-off can be found.

At turn-on the losses are due to the discharge of the total drain capacitance inside the power MOSFET itself. In general, the capacitive losses are given by:

Equation 29

$$P_{cap}(VAC) = \frac{1}{2} \cdot C_d \cdot V^2_{MOS} \cdot f_{sw}(VAC)$$

Where C_d is the total drain capacitance including the MOSFET and the other parasitic capacitances like inductor etc. at the drain node. V_{MOS} is the drain voltage at MOSFET turn-on.

Taking into account the frequency variation with the input line voltage and the phase angle similar to *Equation 29*, a detailed description of the capacitive losses per 1 nF of total drain capacitance can be calculated as:

Equation 30

$$P'_{cap}(VAC) = \frac{1}{2} \cdot \frac{1}{\pi}\int_{\vartheta_1}^{\vartheta 2} \left(2\sqrt{2}VAC - V_{out}\right)^2 f_{sw}(VAC,\vartheta) \cdot d\vartheta$$

θ_1 and θ_2 depend on the input voltage and they are defined below.

Equation 31

$$\vartheta_1 = \arcsin\left(\frac{V_{out}}{2\sqrt{2}VAC}\right)$$

Equation 32

$$\vartheta_2 = \pi - \vartheta_1$$

Figure 5. θ_1 and θ_2 dependence on input voltage

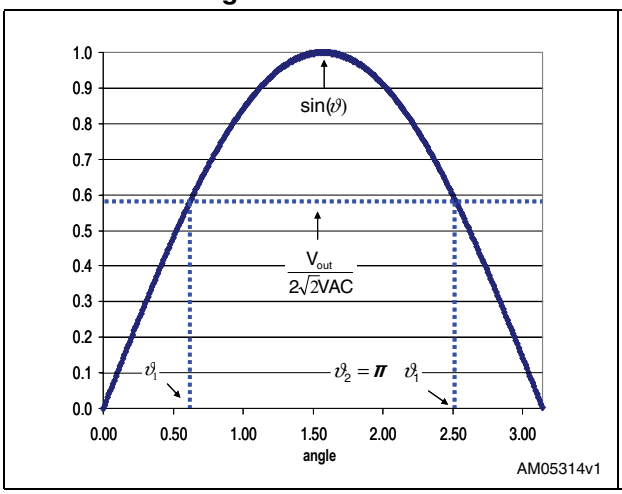
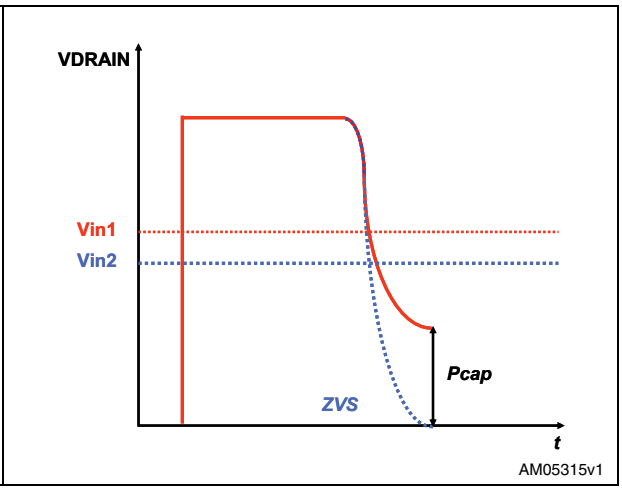


Figure 6. Capacitive losses



The dependence on the input voltage is shown in *Figure 5*. On the right, *Figure 6* represents the drain voltage waveform: the MOSFET turn-on occurs just on the valley because the inductor has depleted its energy and therefore can resonate with the drain capacitance. Details are in the section concerning the ZCD pin description. It is clear that for an input voltage theoretically lower than half of the output voltage, the resonance ideally should reach zero, achieving zero-voltage operation, therefore there are no losses relevant to this edge. For input voltage corresponding to a positive value of the valley, capacitive losses are generated. However, the MOSFET turn-on always occurs at the minimum voltage of the resonance and therefore the losses are minimized.

In practice it is possible to estimate the total switching and capacitive losses by solving the integral of the switching frequency depending on sin(θ) on the half-line cycle.

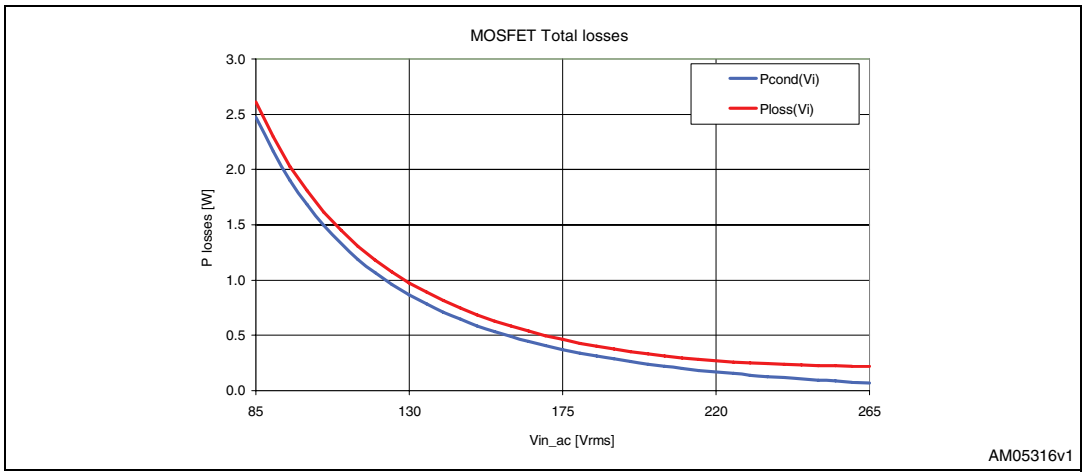
The total losses of the input mains voltage are the sum of the three previous loss functions *Equation 26*, *Equation 28* and *Equation 30* respectively multiplied for the MOSFET parameters:

Equation 33

$$P_{loss}(VAC) = R_{DS(on)} \cdot P'_{cond}(VAC) + \frac{t_{fall}^2}{C_d} \cdot P'_{sw}(VAC) + C_d \cdot P'_{cap}(VAC)$$

Figure 7 shows the trend of the total losses from *Equation 33* on the line voltage for the selected MOSFET STF7NM50N. Capacitive losses are dominant at high mains voltage and the major contribution came from the conduction losses at low and medium mains voltage.

Figure 7. Conduction losses and total losses in the STF7NM50N MOSFET for the L6563S TM PFC



From *Equation 33* using the data relevant to the MOSFET selected, and calculating the losses at VAC_{min} and VAC_{max}, we observe that the maximum total loss occurs at VAC_{min} and is 2.61 W. From this number and the maximum ambient temperature *(12)*, the total maximum thermal resistance required to keep the junction temperature below 125°C is:

Equation 34

$$R_{th} = \frac{125\ °C - T_{ambx}}{P_{loss}(VAC)} \qquad R_{th} = \frac{125\ °C - 50\ °C}{2.58\ W} = 29\frac{°C}{W}$$

If the result of *Equation 34* is lower than the junction-ambient thermal resistance given in the MOSFET datasheet for the selected device package, a heatsink must be used.

For the STF7NM50N the junction - ambient thermal resistance is 62 °C/W, so a heatsink has been used.

3.3.6 Boost diode selection

Following a similar criterion as that used for the MOSFET, the output rectifier can be selected. A minimum breakdown voltage of $1.2 \cdot (Vout + \Delta V_{OVP})$ and current rating higher than $3 \cdot I_{out}$ from *Equation 1* can be chosen for a rough initial selection of the rectifier. The correct choice is then confirmed by the thermal calculation. If the diode junction temperature operates within 125°C, the device has been selected correctly, otherwise a bigger device must be selected.

In this 100 W application an STTH2L06, (600 V, 2 A) has been selected.

The rectifier AVG *Equation 1* and RMS *Equation 8* current values and the parameter V_{th} (rectifier threshold voltage) and R_d (dynamic resistance) given in the datasheet allow calculating the rectifier losses.

From the STTH2L06 datasheet, V_{th} is 0.89 V, R_d is 0.08 Ω

Equation 35

$$P_{diode} = V_{th} \cdot I_{out} + R_d \cdot ID^2_{rms} \qquad P_{diode} = 0.89\ V \cdot 0.25\ A + 0.08\ \Omega \cdot (0.72\ A)^2 = 0.26\ W$$

From *(12)* and *Equation 35* the maximum thermal resistance to keep the junction temperature below 125 °C is:

Equation 36

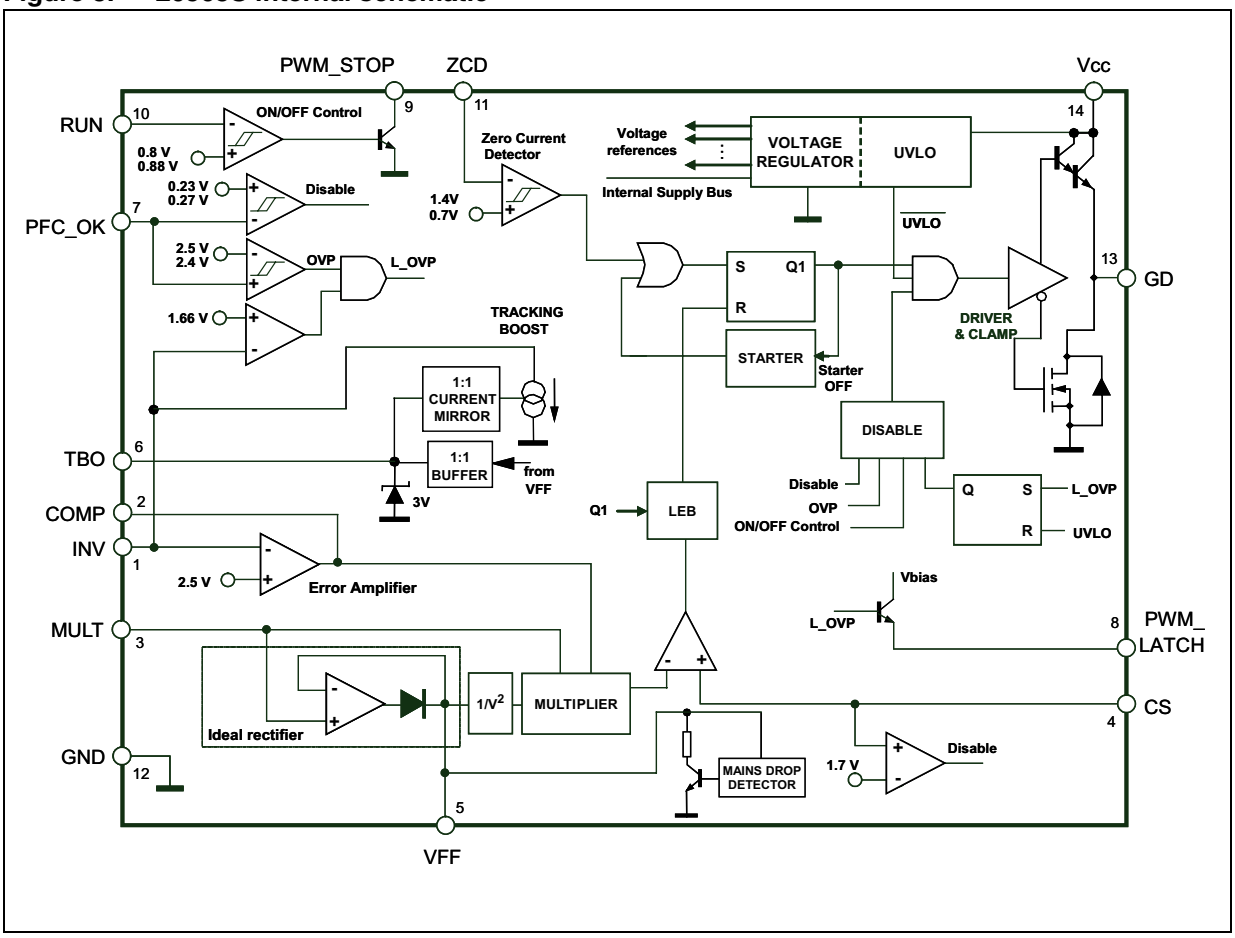
$$R_{th} = \frac{125\,°C - T_{ambx}}{P_{diode}} \qquad R_{th} = \frac{125°C - 50°C}{0.26\,W} = 284.68\frac{°C}{W}$$

Because the calculated R_{th} is lower than the STTH2L06 thermal resistance junction-ambient, a heatsink is not needed to properly dissipate the heat.

3.4 L6563S biasing circuitry

In this section we describe the dimensioning of the power components as well as the biasing circuitry for the L6563S. For reference, the internal schematic of the L6563S is represented below in *Figure 8*. For more details on the internal functions please refer to the datasheet.

Figure 8. L6563S internal schematic



Pin 1 (INV): This pin is connected both to the inverting input of the E/A and to the OVP circuitry. A resistive divider has to be connected between the boost regulated output voltage and this pin. The internal reference on the E/A non-inverting input is 2.5 V (typ.). The PFC output voltage (Vout) is set at its nominal value by the resistor ratio of the feedback output divider. R_{outH} and R_{outL} are then selected considering the nominal output voltage *(4)* and

the desired output power dissipated on the output divider. For example, considering a power dissipation of 50 mW:

Equation 37

$$R_{outH} = \frac{(V_{OUT} - 2.5V)^2}{50\ mW} \qquad R_{outH} = \frac{(400\ V - 2.5\ V)^2}{50\ mW} = 3.160\ M\Omega$$

With the commercial resistor selected, R_{outH} = 3 MΩ

Equation 38

$$\frac{R_{outH}}{R_{outL}} = \frac{V_{out}}{2.5\ V} - 1 \qquad \frac{R_{outH}}{R_{outL}} = \frac{400\ V}{2.5\ V} - 1 = 159$$

Equation 39

$$R_{outL} = \frac{R_{outH}}{159} \qquad R_{outL} = \frac{3\ M\Omega}{159} = 18.8\ k\Omega$$

The R_{outL} = 62 kΩ resistor in parallel to 27 kΩ has been selected for giving a total resistance close to the calculated value. Please note that for R_{outH} a resistor with a suitable voltage rating (>400 V) is needed, or more resistors in series have to be used.

Please note also that the maximum value of the resistor divider is limited by the L6563S INV pin input bias current given in the datasheet. To guarantee correct output voltage regulation, the current flowing in the resistor divider must be significantly higher than the current flowing into the pin.

Pin 7 (PFC_OK - feedback failure protection): the PFC_OK pin has been dedicated to monitor the output voltage with a separate resistor divider. This divider is selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset value V_{OVP} *(7)*, usually larger than the maximum Vout that can be expected, also including worst-case load/line transients. For a maximum output voltage Vout max of 430 V and imaging a 50 µA current flowing into the divider:

Equation 40

$$R_L = \frac{V_{REF_PFC_OK}}{I_{divider}} \qquad R_L = \frac{2.5\ V}{50\ \mu A} = 50\ k\Omega$$

By selecting a commercial resistor of 51 kΩ:

Equation 41

$$R_H = R_L \cdot \left(\frac{V_{OUT_MAX}}{V_{REF_PFC_OK}} - 1 \right) \qquad R_H = 51\,k\Omega \cdot \left(\frac{430\ V}{2.5\ V} - 1 \right) = 8.721\,M\Omega$$

Using two 3.3 MΩ resistors and one 2.2 MΩ resistor, a total output PFC_OK high resistor of 8.8 MΩ has been obtained.

Notice that both feedback dividers connected to L6563S pin #1 (INV) and pin #7 (PFC_OK) can be selected without any constraints. The unique criterion is that both dividers have to sink a current from the output bus which needs to be significantly higher than the current biasing the error amplifier and PFC_OK comparator.

The OVP function described above is able to handle “normal” overvoltage conditions, i.e. those resulting from an abrupt load/line change or occurring at startup. In case the

overvoltage is generated by a feedback disconnection, for instance, when one of the upper resistors of the output divider fails open, an additional circuitry detects the voltage drop of pin INV. If the voltage on pin INV is lower than 1.66 V (Typ.) and at same time the OVP is active, a feedback failure is assumed. Thus, the gate drive activity is immediately stopped, the device is shut down, its quiescent consumption is reduced below 180 µA and the condition is latched as long as the supply voltage of the IC is above the UVLO threshold. To restart the system it is necessary to recycle the input power, so that the Vcc voltage of the L6563S goes below 6 V and that one of the PWM controller goes below its UVLO threshold. Note that this function offers a complete protection against not only feedback loop failures or erroneous settings, but also against a failure of the protection itself. Either resistor of the PFC_OK divider failing short or open or a floating PFC_OK pin results in shutting down of the IC and stopping the pre-regulator. Moreover, the pin PFC_OK doubles its function as a non-latched IC disable. A voltage below 0.23 V shuts down the IC, reducing its consumption below 2 mA. To restart the IC simply let the voltage at the pin go above 0.27 V.

Pin 2 (COMP): This pin is the output of the E/A that is fed to one of the two inputs of the multiplier. A feedback compensation network is placed between this pin and INV (pin #1). It has to be designed with a narrow bandwidth in order to avoid that the system rejects the output voltage ripple (100 Hz) that would lead to a high distortion of the input current waveform.

A simple criterion to define the capacitance value is to set the bandwidth (BW) from 20 to 30 Hz. The compensation network can be just a capacitor, providing a low-frequency pole as well as a high DC gain. A more complex network, typically a type-II CRC network providing 2 poles and a zero, is more suitable for constant power loads like a downstream converter.

In case a single capacitor is used, it can be dimensioned using the following formulas:

Equation 42

$$BW = \frac{1}{2\pi \cdot (R_{outH} // R_{outL}) \cdot C_{Compensation}}$$

Equation 43

$$C_{Compensation} = \frac{1}{2\pi \cdot (R_{outH} // R_{outL}) \cdot BW}$$

For a more complex compensation network calculation, please refer to [2], [3].

For this 100 W TM PFC, a CRC network providing two poles and a zero has been implemented here, using the following values:

$$C_{compP} = 68\ nF \quad C_{compS} = 680\ nF \quad R_{compS} = 82\ k\Omega \qquad (14)$$

The relevant open loop transfer function and its phase function are shown in *Figure 9* and *Figure 10*.

Figure 9. Open loop tran. function bode plot

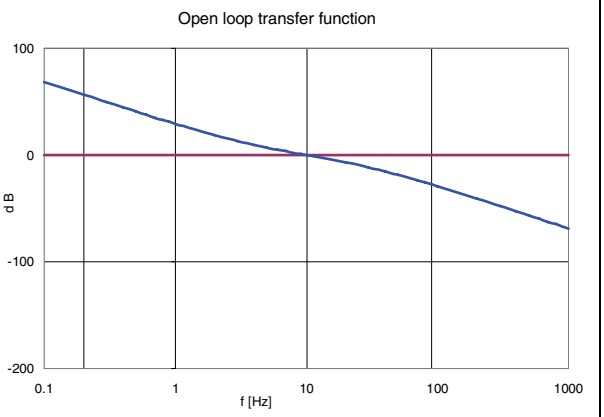
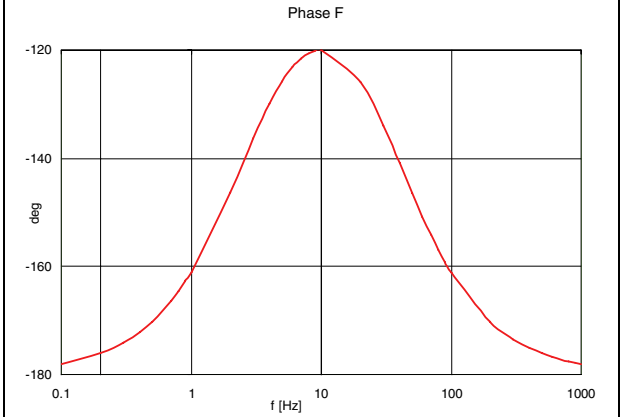


Figure 10. Phase function



The two bode plot charts refer to the PFC operating at 265Vac and full load. In this condition the crossover frequency is f_c = 11.55 Hz, the phase margin is 55°. The third harmonic distortion introduced by the E/A 100 Hz residual ripple is below 3%.

Pin 4 (CS): The pin #4 is the inverting input of the current sense comparator. Through this pin, the L6563S reads the instantaneous inductor current, converted to a proportional voltage by an external sense resistor (R_s). As this signal crosses the threshold set by the multiplier output, the PWM latch is reset and the power MOSFET is turned off. The MOSFET stays in an off-state until the PWM latch is set again by the ZCD signal. The pin is equipped with 150 ns leading-edge blanking for improved noise immunity.

The sense resistor value (R_s) can be calculated as follows. For the 100 W PFC it is:

Equation 44

$$R_s < \frac{Vcs_{min}}{IL_{pk}} \qquad R_s < \frac{1.0\ V}{3.38\ A} = 0.296\ \Omega$$

where:

- IL_{pk} is the maximum peak current in the inductor, calculated as described in *Equation 4*
- Vcs_{min} = 1.0 V, and is the minimum voltage admitted on the L6563S current sense (in the datasheet)

Because the internal current sense clamping sets the maximum current that can flow in the inductor, the maximum peak of the inductor current is calculated considering the maximum voltage Vcs_{max} admitted on the L6563S (in the datasheet):

Equation 45

$$IL_{pkx} = \frac{Vcs_{max}}{R_s} \qquad IL_{pkx} = \frac{1.16\ V}{0.27\ \Omega} = 4.30\ A$$

The calculated IL_{pkx} is the threshold value after which the boost inductor saturates and it is used for calculating the inductor number of turns and air gap length. In case of boost inductor saturation, a second comparison level at 1.7 V detects the abnormal currents and, on this occurrence, activates a safety procedure that temporarily stops the converter and limits the stress of the power components.

The power dissipated in R_s is given by:

Equation 46

$$P_s = R_s \cdot ISW_{rms}^2 \quad P_s = 0.27\ \Omega \cdot (1.18\ A)^2 = 0.37\ W$$

According to the result, two parallel resistors of 0.47 Ω and 0.68 Ω with 0.25 W of power have been selected.

Pin 3 (MULT): The MULT pin is the second multiplier input. It is connected, through a resistive divider, to the rectified mains to get a sinusoidal voltage reference. The multiplier can be described by the relationship:

Equation 47

$$V_{CS} = V_{CS_OFFSET} + k_m \cdot \frac{(V_{COMP} - 2.5\ V) \cdot V_{MULT}}{V_{FF}^2}$$

where:

- V_{CS} (multiplier output) is the reference for the current sense (V_{CS_OFFSET} is its offset)
- k = 0.45 (typ.) is the multiplier gain
- V_{COMP} is the voltage on pin #2 (E/A output)
- V_{MULT} is the voltage on pin #3.
- V_{FF} is the second input to the multiplier for the $1/V^2$ function. It compensates the control loop gain dependence on the mains voltage. The voltage at this pin is a DC level equal to the peak voltage on pin MULT (pin #3).

Figure 11. Multiplier characteristics family for V_{FF} = 1 V

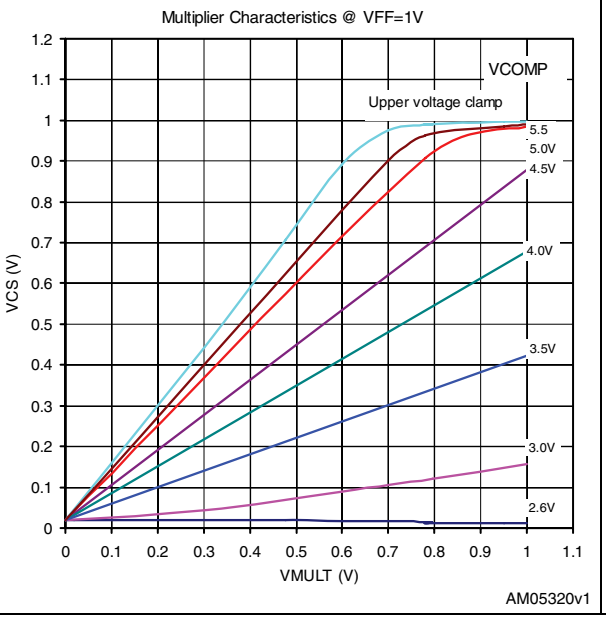
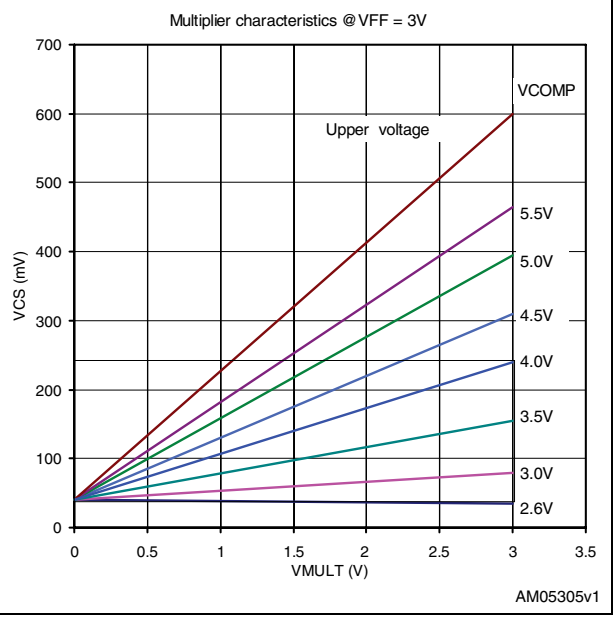


Figure 12. Multiplier characteristics family for V_{FF} = 3 V



A complete description is given by the diagrams of *Figure 11* and *Figure 12* which show the typical multiplier characteristics family. The linear operation of the multiplier is guaranteed

within the range 0 to 3 V of V_{MULT} and the range 0 to 1.16 V (typ.) of V_{CS}, while the minimum guaranteed value of the maximum slope of the characteristics family (typ.) is:

Equation 48

$$\frac{dV_{CS}}{dV_{MULT}} = 1.66\frac{V}{V}$$

The voltage on the MULT pin is also used to derive the information from the RMS mains voltage for the V_{FF} compensation.

We suggest the following procedure to properly set the operating point of the multiplier. First, the maximum peak value for V_{MULT}, $VMULT_{max}$ is selected. This value, which occurs at maximum mains voltage, should be 3 V or nearly so in wide-range mains and less in case of single mains. The sense resistor selected is R_s = 0.27 Ω as given in *Equation 44*. According to the L6563S datasheet and to the linearity setting of the pin, the maximum voltage accepted on the multiplier input is:

$$VMULT_{max} = 3\ V \quad (15)$$

where IL_{pk} and R_s have been already calculated, 1.66 is the multiplier maximum slope given in the datasheet.

From *(15)* the maximum required divider ratio is calculated as:

Equation 49

$$k_p = \frac{V_{MULT\,max}}{\sqrt{2}\cdot VAC_{max}} = \frac{3.00\ V}{\sqrt{2}\cdot 265Vac} = 8\cdot 10^{-3}$$

Supposing a 60 µA current flowing into the multiplier divider, the lower resistor value can be calculated:

Equation 50

$$R_{multL} = \frac{V_{MULT\,max}}{60\ \mu A} = \frac{3.00\ V}{60\ \mu A} = 50\ k\Omega$$

A commercial resistor of 51 kΩ for the lower resistor is selected. The upper resistor value can now be calculated as:

Equation 51

$$R_{multH} = \frac{1-k_p}{k_p}R_{multL} = \frac{1-8\cdot 10^{-3}}{8\cdot 10^{-3}}51\,k\Omega = 6.319\ M\Omega$$

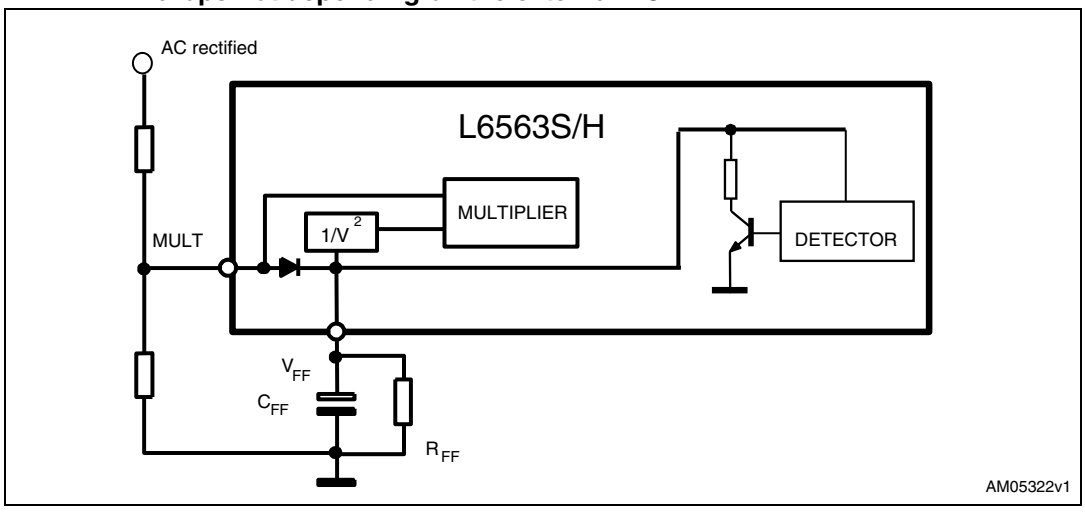
In this application example R_{multH} = 6.6 MΩ and R_{multL} = 51 kΩ have been selected. Please note that for R_{multH} a resistor with a suitable voltage rating (>400 V) is needed, or more resistors in series must be used.

The voltage on the multiplier pin with the selected component values is re-calculated at minimum line voltage (0.93 V) and at maximum line voltage (2.74 V). So the multiplier works correctly within its linear region.

Pin 5 (voltage feed-forward): The power stage gain of PFC pre-regulators varies with the square of the RMS input voltage as well as the crossover frequency f_c of the overall open-loop gain because the gain has a single pole characteristic. This leads to large trade-offs in

the design. For example, setting the gain of the error amplifier to get f_c = 20 Hz at 264 Vac means having f_c = 4 Hz at 88 Vac, resulting in a sluggish control dynamics. Additionally, the slow control loop causes large transient current flow during rapid line or load changes that are limited by the dynamics of the multiplier output. This limit is considered when selecting the sense resistor to let the full load power pass under minimum line voltage conditions, with some margin. But a fixed current limit allows excessive power input at high line, whereas a fixed power limit requires the current limit to vary inversely with the line voltage. Voltage feed-forward can compensate for the gain variation with the line voltage and allow overcoming all of the above-mentioned issues. It consists of deriving a voltage proportional to the input RMS voltage, feeding this voltage into a square/divider circuit ($1/V^2$ corrector) and providing the resulting signal to the multiplier that generates the current reference for the inner current control loop (*Figure 13*). In this way a change of the line voltage causes an inversely proportional change of the half sine amplitude at the output of the multiplier (if the line voltage doubles, the amplitude of the multiplier output is halved and vice-versa) so that the current reference is adapted to the new operating conditions with (ideally) no need for invoking the slow dynamics of the error amplifier. Additionally, the loop gain is constant throughout the input voltage range, which improves significantly dynamic behavior at low line and simplifies loop design. Actually, deriving a voltage proportional to the RMS line voltage implies a form of integration, which has its own time constant. If it is too small the voltage generated is affected by a considerable amount of ripple at twice the mains frequency that causes distortion of the current reference (resulting in high THD and poor PF); if it is too large there is a considerable delay in setting the right amount of feedforward, resulting in excessive overshoot and undershoot of the pre-regulator's output voltage in response to large line voltage changes. Clearly a trade-off is required. The device implements voltage feed-forward with a technique that makes use of just two external parts and that limits the feed-forward time constant trade-off issue to only one direction.

Figure 13. Mains detector and discharge resistor allow fast response to sudden line drops not depending on the external RC



A capacitor C_{FF} and a resistor R_{FF}, both connected from the V_{FF} (pin #5) pin to ground, complete an internal peak-holding circuit that provides a DC voltage equal to the peak of the rectified sine wave applied on pin MULT (pin #3). In case the V_{FF} pin is connected directly to the RUN pin, the following values are suggested as a compromise between the response time in case of mains transients and input current distortion:

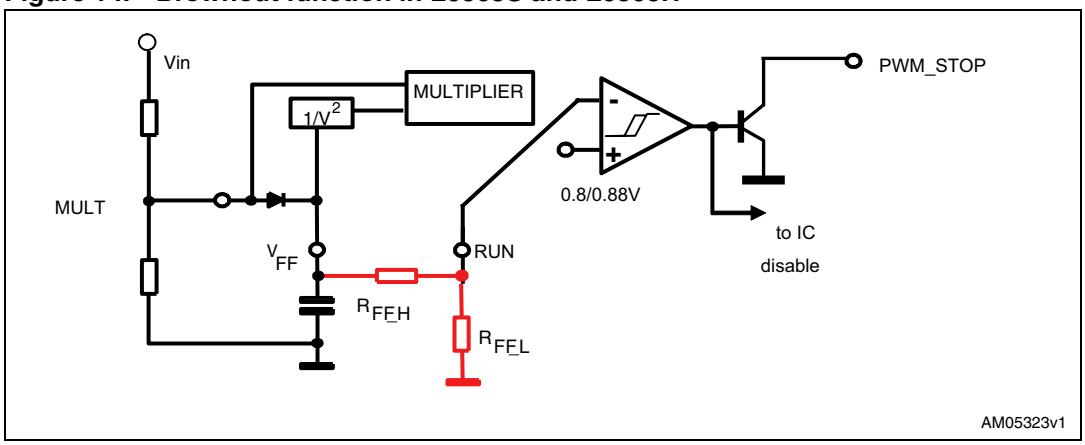
$$C_{FF} = 1\,\mu F \qquad R_{FF} = 1\,M\Omega \tag{16}$$

In this way, in case of sudden line voltage rise, C_{FF} is rapidly charged through the low impedance of the internal diode and no appreciable overshoot is visible at the pre-regulator's output. In case of a line voltage drop, an internal “mains drop” detector enables a low impedance switch which suddenly discharges C_{FF} avoiding long settling time before reaching the new voltage level. Consequently an acceptably low steady-state ripple and low current distortion can be achieved without any considerable undershoot or overshoot on the preregulator's output like in systems with no feed-forward compensation.

Pin 10 (RUN): Remote ON/OFF control. A voltage below 0.8 V shuts down (does not latch) the IC and brings its consumption to a considerably lower level. PWM_STOP is asserted low. The IC restarts as the voltage at the pin goes above 0.88 V.

The brownout function can be easily implemented by connecting the RUN pin through a divider to the V_{FF} pin as shown in the *Figure 14*.

Figure 14. Brownout function in L6563S and L6563H



The divider replaces the discharge resistor R_{FF} shown in *Figure 13*. It should be selected in order to have a similar time constant of *(16)* but also to obtain the PFC startup at minimum input mains voltage VAC_{min} (in this design 90Vac) as specified in *(1)*.

Thus, we can set:

$$C_{FF} = 1\,\mu F \qquad (17)$$

Referring to *Figure 14* and considering the peak of the minimum input mains voltage, the corresponding voltage on the V_{FF} pin is:

Equation 52

$$V_{FF@V_{START}} = \sqrt{2} \cdot V_{START} \cdot \frac{R_{multL}}{R_{multL} + R_{multH}} - \Delta V$$

$$V_{FF@V_{START}} = \sqrt{2} \cdot 90Vac \cdot \frac{51k\Omega}{51\,k\Omega + 6.6\,M\Omega} - 20\,mV = 0.973\,V$$

ΔV is the voltage drop between the V_{FF} and MULT pins.

Now, considering the RUN pin enable threshold (0.88 V is the typical value given in the datasheet), the RUN pin divider ratio can be calculated as follows:

Equation 53

$$\frac{V_{RUN_EN}}{V_{FF@V_{START}}} = \frac{R_{FF_L}}{R_{FF_L} + R_{FF_H}} = 0.904$$

Setting up R_{FF_L} = 1 MΩ, R_{FF_H} can be calculated from *Equation 53*.

Equation 54

$$R_{FF_H} = \left(\frac{V_{FF@V_{START}}}{V_{RUN_EN}} - 1\right) \cdot R_{FF_L} \qquad R_{FF_H} = \left(\frac{0.973\ V}{0.88\ V} - 1\right) \cdot 1M\Omega = 105\ k\Omega$$

The result of *Equation 54* is based on typical values and doesn't take into account the V_{RUN_EN} threshold and the resistor tolerances. In order to have the startup at minimum mains voltage as set in *(1)* and guarantee against variation of parameters, the mentioned tolerances should be taken into account, making calculations to consider the worst cases.

In this case, taking into account the resistors and threshold tolerances, 1 MΩ and 56 kΩ have been calculated, thus the actual divider ratio is 0.946. Then the following check can be done:

Equation 55

$$V_{FF_ENABLE} = V_{RUN_EN} \cdot \frac{R_{FF_L} + R_{FF_H}}{R_{FF_L}} \qquad V_{FF_ENABLE} = 0.88\ V \cdot \frac{1M\Omega + 56\ k\Omega}{1M\Omega} = 0.923\ V$$

Equation 56

$$V_{in_START} = \left(\frac{V_{FF_EN} + 20mV}{\sqrt{2}}\right) \cdot \frac{R_{multH} + R_{multL}}{R_{multL}}$$

$$V_{in_START} = \left(\frac{0.923\ V + 20\ mV}{\sqrt{2}}\right) \cdot \frac{6.6\ M\Omega + 51\ k\Omega}{51\ k\Omega} = 87Vac$$

Equation 57

$$V_{FF_DISABLE} = V_{RUN_DIS} \cdot \frac{R_{FF_L} + R_{FF_H}}{R_{FF_L}} \qquad V_{FF_DISABLE} = 0.80\ V \cdot \frac{1M\Omega + 56\ k\Omega}{1M\Omega} = 0.844\ V$$

Equation 58

$$V_{in_STOP} = \left(\frac{V_{FF_DIS} + 20\ mV}{\sqrt{2}}\right) \cdot \frac{R_{multH} + R_{multL}}{R_{multL}}$$

$$V_{in_STOP} = \left(\frac{0.844\ V + 20\ mV}{\sqrt{2}}\right) \cdot \frac{6.6\ M\Omega + 51\ k\Omega}{51\ k\Omega} = 79.9Vac$$

Pin 11 (ZCD): The pin #11 is the input of the zero-current detector circuit. In transition-mode PFC the ZCD pin is connected, through a limiting resistor, to the auxiliary winding of the boost inductor. The ZCD circuit is negative-going edge triggered. When the voltage on the pin falls below 0.7 V, it sets the PWM latch and thus the MOSFET is turned on. To do so the circuit must first be armed. Prior to falling below 0.7 V, the voltage on pin #5 must experience a positive-going edge exceeding 1.4 V (due to the MOSFET's turn-off). The maximum main-to-auxiliary winding turn ratio, nmax, has to ensure that the voltage delivered to the pin

during the MOSFET's off-time is sufficient to arm the ZCD circuit. A safe margin of 15% is added.

Equation 59

$$nmax = \frac{n_{primary}}{n_{auxiliary}} = \frac{V_{out} - \sqrt{2} \cdot VAC_{max}}{1.4\ V \cdot 1.15} \qquad nmax = \frac{400\ V - \sqrt{2} \cdot 265Vac}{1.4\ V \cdot 1.15} = 15.71$$

If the winding is also used for supplying the IC, the above criterion may not be compatible with the Vcc voltage range. To solve this incompatibility the self-supply network shown in the schematic of *Figure 28*, *Figure 29* can be used.

The minimum value of the limiting resistor can be found considering the maximum voltage across the auxiliary winding with a selected turn ratio of 10 and assuming 0.6 mA current through the pin.

Equation 60

$$R_1 = \frac{\frac{V_{out}}{n_{aux}} - V_{ZCDH}}{0.6\ mA} \qquad R_1 = \frac{\frac{400\ V}{10} - 5.7\ V}{0.6\ mA} = 57.16\ k\Omega$$

Equation 61

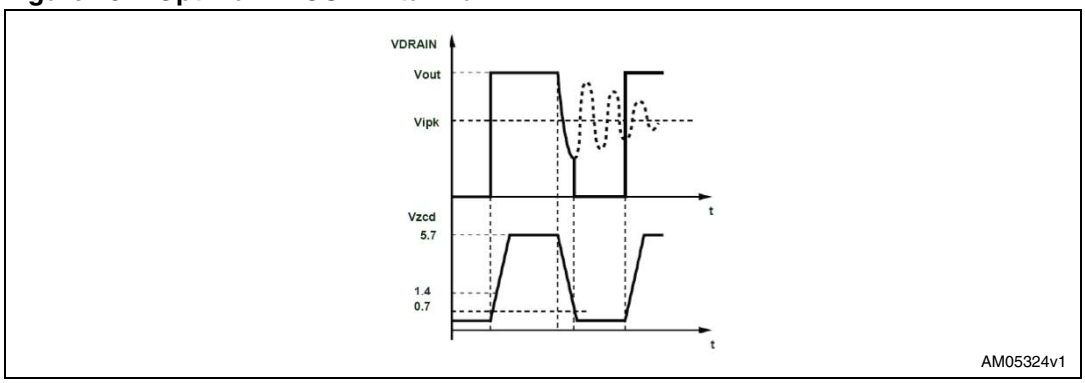
$$R_2 = \frac{\frac{\sqrt{2} \cdot VAC_{max}}{n_{aux}} - V_{ZCDL}}{0.6\ mA} \qquad R_2 = \frac{\frac{\sqrt{2} \cdot 265Vac}{10} - 0\ V}{0.6\ mA} = 62.4\ k\Omega$$

V_{ZCDH} = 5.7 V and V_{ZCDL} = 0 V are the upper and lower ZCD clamp voltages of the L6563S.

Considering the higher value between the two calculated, an R_{ZCD} = 68 kΩ has been selected as the limiting resistor.

The actual value can then be fine-tuned in order to make the turn-on of the MOSFET occur just on the valley of the drain voltage (which is resonating because the boost inductor has run out of energy, (*Figure 15*).This minimizes the power dissipation at turn-on.

Figure 15. Optimum MOSFET turn-on



Pin 6 (TBO): In some applications it may be advantageous to regulate the output voltage of the PFC preregulator so that it tracks the RMS input voltage rather than at a fixed value like in conventional boost pre-regulators. This is commonly referred to as a “tracking boost” or “follower boost” approach.

With this IC the function can be implemented by connecting a resistor (R_T) between the TBO pin and ground. The TBO pin presents a DC level equal to the peak of the MULT pin voltage and is then representative of the mains RMS voltage. The resistor defines a current, equal to V(TBO)/R_T, that is internally 1:1 mirrored and sunk from pin INV (pin #1) input of the error amplifier. In this way, when the mains voltage increases, the voltage at TBO pin increases as well which increases the current flowing through the resistor connected between TBO and GND. Then a larger current is sunk by the INV pin and the output voltage of the PFC preregulator is forced to go higher. Obviously, the output voltage moves in the opposite direction if the input voltage decreases. To avoid undesired output voltage rise should the mains voltage exceed the maximum specified value, the voltage at the TBO pin is clamped at 3 V. By properly selecting the multiplier bias it is possible to set the maximum input voltage above which input-to-output tracking ends and the output voltage becomes constant. If this function is not used, leave the pin open: the device regulates a fixed output voltage.

Starting from the following data:

- Minimum specified input RMS voltage V_{in1} (18)
- Maximum specified input RMS voltage V_{in2} (19)
- Regulated output voltage at $V_{in} = V_{in1}$ V_{o1} (20)
- Regulated output voltage at $V_{in} = V_{in2}$ V_{o2} (21)
- Absolute maximum limit for the regulated output voltage V_{ox} (22)
- Maximum output voltage (Vdc) - *(7)* V_{OVP} (23)

To set the output voltage at the desired values use the following design procedure:

1. Determine the input RMS voltage $V_{inCLAMP}$ that produces Vo = V_{ox}:

Equation 62

$$V_{inCLAMP} = \frac{V_{OX} - V_{O1}}{V_{O2} - V_{O1}} \cdot V_{in2} - \frac{V_{OX} - V_{O2}}{V_{O2} - V_{O1}} \cdot V_{in1}$$

and choose a value V_{inx} such that $V_{in2} = V_{inx} < V_{inCLAMP}$. This results in a limitation of the output voltage range below V_{ox} (it equals V_{ox} if one chooses $V_{inx} = V_{inCLAMP}$)

2. Determine the divider ratio of the MULT pin (pin #3) bias:

Equation 63

$$k = \frac{3}{\sqrt{2} \cdot V_{inx}}$$

and check that at minimum mains voltage V_{in1} the peak voltage on pin #3 is greater than 0.9 V.

3. Determine R_{outH}, the upper resistor of the output divider, for instance 3 MΩ

$$R_{outH} \qquad (24)$$

4. Calculate the lower resistor R_{outL} of the output divider and the adjustment resistor R_T:

Equation 64

$$R_{outL} = 2.5\ V \cdot R_{outH} \frac{V_{in2} - V_{in1}}{(V_{O1} - 2.5\ \ V) \cdot V_{in2} - (V_{O2} - 2.5\ V) \cdot V_{in1}}$$

Equation 65

$$R_T = k \cdot \sqrt{2} \cdot R_{outH} \cdot \frac{V_{in2} - V_{in1}}{V_{O2} - V_{O1}}$$

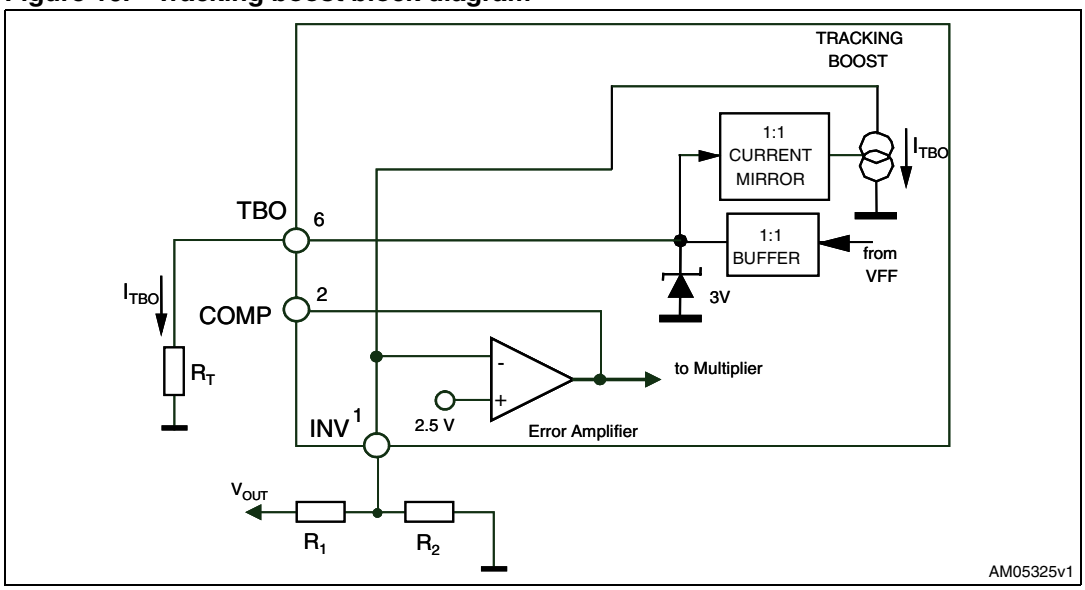
5. Check that the maximum current sourced by the TBO pin (pin #6) does not exceed the maximum specified (0.25 mA):

Equation 66

$$I_{TBOmax} = \frac{3}{R_T}$$

The circuit illustrated in *Figure 16* shows the internal block diagram of the tracking boost function.

Figure 16. Tracking boost block diagram



Note that in this design example of the 100 W board PFC, the tracking boost function has not been used because the PFC has to supply a stable 400 V output voltage over the entire input mains.

Pin 8 (PWM_LATCH): Output pin for fault signaling. During normal operation this pin features high impedance. If a feedback failure is detected (PFC_OK > 2.5 V and INV+40 mV < PFC_OK) the pin is asserted high. Normally, this pin is used to stop the operation of the DC-DC converter supplied by the PFC pre-regulator by invoking a latched disable of its PWM controller. If not used, the pin is left floating.

Pin 9 (PWM_STOP): Output pin for fault signaling. During normal operation this pin features high impedance. If the IC is disabled by a voltage below 0.8 V on pin RUN (#10), the voltage on the pin is pulled to ground. Normally, this pin is used to temporarily stop the operation of the DC-DC converter supplied by the PFC pre-regulator by disabling its PWM controller. A typical usage of this function is brownout protection in systems where the PFC pre-regulator is the master stage. If not used, the pin is left floating.

Pin 12 (GND): This pin acts as the current return both for the signal internal circuitry and for the gate drive current. When laying out the printed circuit board, these two paths should run separately.

Pin 13 (GD): is the output of the driver. The pin is able to drive an external MOSFET with 600 mA source and 800 mA sink capability.

The high-level voltage of this pin is clamped at about 12 V to avoid excessive gate voltages in case the pin is supplied with a high Vcc. To avoid undesired switch-on of the external MOSFET because of some leakage current when the supply of the L6563S is below the UVLO threshold, an internal pull-down circuit holds the pin low. The circuit guarantees 1.1 V maximum on the pin (at I_{sink} = 2 mA), with $V_{cc} > V_{CC_ON}$. This allows omitting the “bleeder” resistor connected between the gate and the source of the external MOSFET used for this purpose.

Pin 14 (Vcc): is the supply of the device. This pin is externally connected to the startup circuit (usually, one resistor connected to the rectified mains) and to the self-supply circuit.

Whatever the configuration of the self-supply system, a capacitor is connected between this pin and ground.

To start the L6563S, the voltage must exceed the startup threshold (12 V typ.). Below this value the device does not work and consumes less than 90 µA (typ.) from Vcc. This allows the use of high value startup resistors (in the hundreds of kΩ), which reduces power consumption and optimizes system efficiency at low load, especially in wide-range mains applications.

When operating, the current consumption (of the device only, not considering the gate drive current) rises to a value depending on the operating conditions but never exceeding 6 mA.

The device keeps working as long as the supply voltage is over the UVLO threshold (13 V max). If the Vcc voltage exceeds 22.5 V, an internal Zener diode, 20 mA rated, is activated in order to clamp the voltage. Please remember that during normal operation the internal Zener does not have to clamp the voltage, because in that case the power consumption of the device increases considerably and its junction temperature increases too. The suggested operating condition for safe operation of the device is below the minimum clamping voltage of the pin.

4 L6563H: high-voltage startup transition-mode PFC

The L6563H is a new current-mode PFC controller operating in transition mode (TM) which embeds the same features existing in the L6563S with the addition of a high-voltage startup. The package and pinout of the two devices are different as shown in *Figure 17* and *Figure 18*. The pin function is the same, in this paragraph a detailed description of the HV startup system is given.

Figure 17. L6563H - SO16

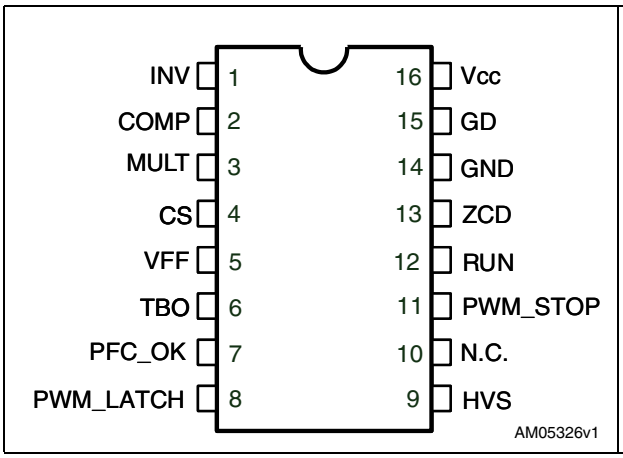


Figure 18. L6563S - SO14

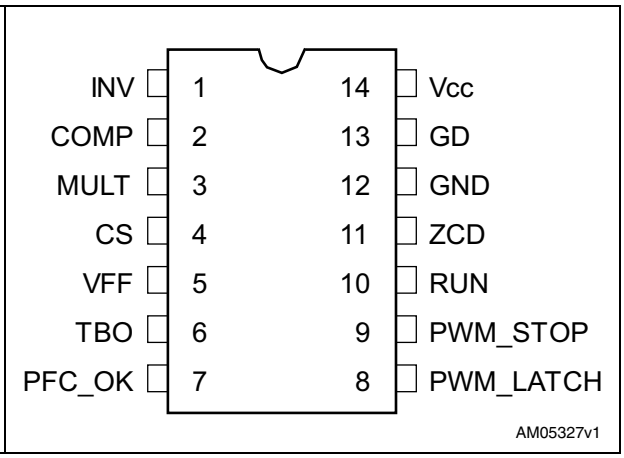
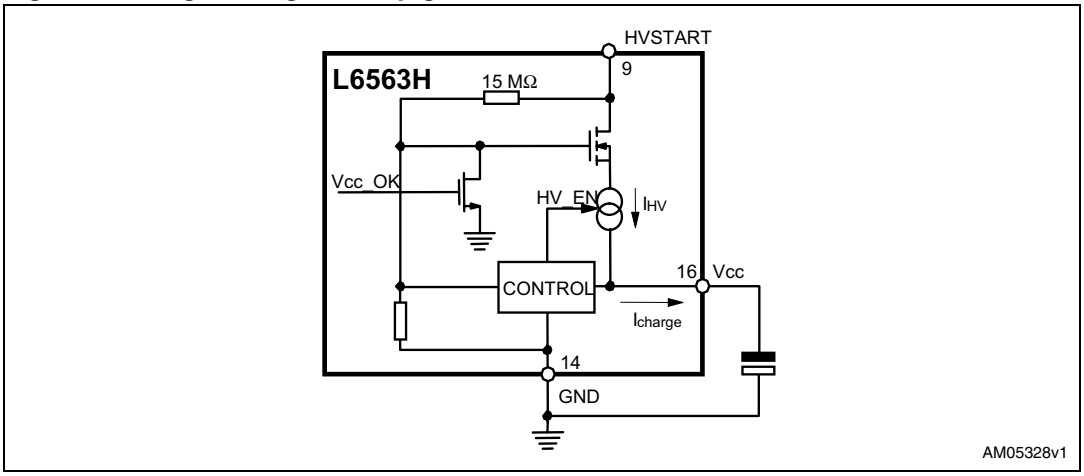


Figure 19 shows the internal schematic of the high-voltage startup generator. It is made up of a high-voltage N-channel FET, whose gate is biased by a 15 MΩ resistor, with a temperature-compensated current generator connected to its source.

The HV generator is physically located on a separate chip, made with BCD off-line technology able to withstand 700 V, controlled by a low-voltage chip, where all of the control functions reside.

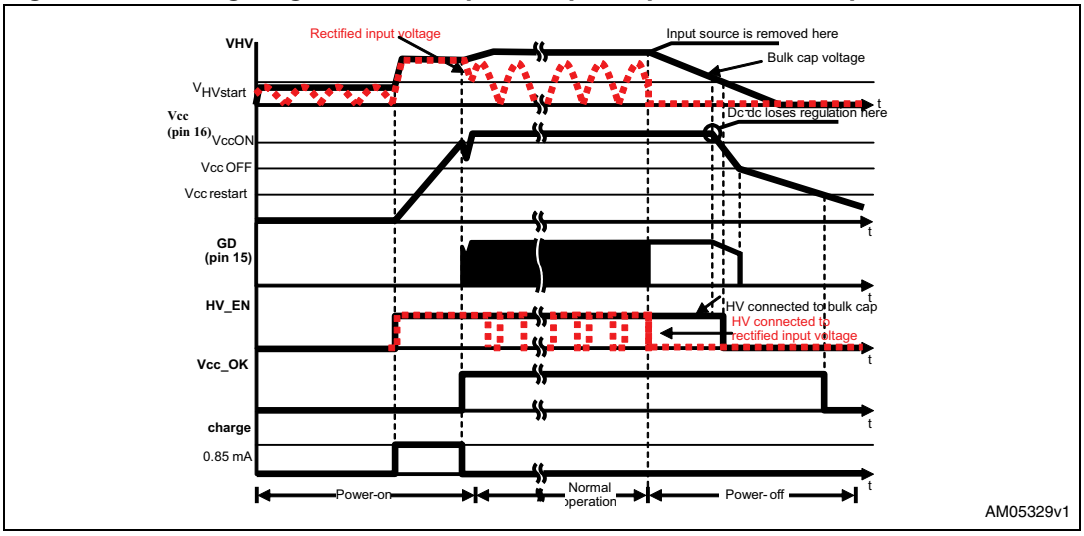
Figure 19. High-voltage startup generator: internal schematic



With reference to the timing diagram of *Figure 20*, when power is first applied to the converter the voltage on the bulk capacitor (V_{in}) builds up and, at about 80 V, the HV generator is enabled to operate (HV_EN is pulled high) so that it draws about 1 mA. This

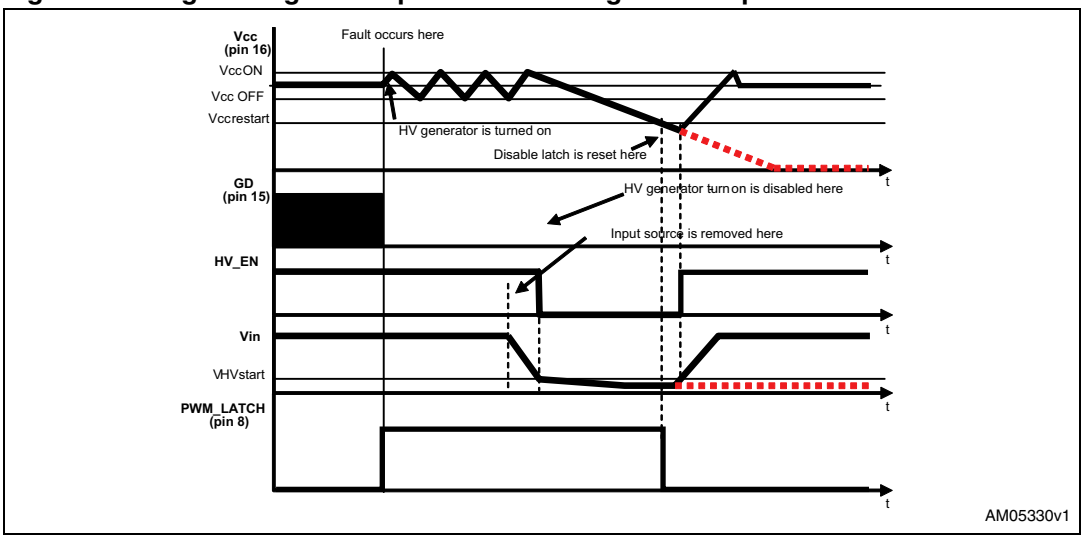
current, minus the device's consumption, charges the bypass capacitor connected from pin Vcc to ground and makes its voltage rise almost linearly.

Figure 20. Timing diagram: normal power-up and power-down sequences



As the Vcc voltage reaches the startup threshold (12 V typ.) the low-voltage chip starts operating and the HV generator is cut off by the Vcc_OK signal asserted high. The device is powered by the energy stored in the Vcc capacitor until the self-supply circuit (assuming that it is made with an auxiliary winding in the transformer of the cascaded DC-DC converter and a steering diode) develops a voltage high enough to sustain the operation. The residual consumption of this circuit is only the one on the 15 MΩ resistor (10 mW at 400 Vdc), typically 50-70 times lower, under the same conditions, as compared to a standard startup circuit made with external resistors. At converter power-down the DC-DC converter loses regulation as soon as the input voltage is so low that either peak current or maximum duty cycle limitation is tripped. Vcc then drops and stop IC activity as it falls below the UVLO threshold (9.5 V typ.). The Vcc_OK signal is de-asserted as the Vcc voltage goes below a threshold $VCC_{restart}$ located at about 6 V. The HV generator can now restart. However, if $V_{in} < V_{HVstart}$, HV_EN is de-asserted too and the HV generator is disabled. This prevents the converter's restart attempts and ensures monotonic output voltage decay at power-down in systems where brownout protection (see the relevant section) is not used. If the device detects a fault due to feedback failure, the pin PWM_LATCH is asserted high (see “feedback failure protection” section for more details) and, in order to maintain this signal to be provided to the DC-DC converter, the internal $VCC_{restart}$ is brought up above Vcc_{Off} (turn-off threshold).

Figure 21. High-voltage startup behavior during latch-off protection



As a result, shown in *Figure 21*, the voltage at pin Vcc oscillates between its turn-on and turn-off thresholds until the HV bus is recycled and drops below the startup threshold of the HV generator. The high-voltage startup circuitry is capable of guaranteeing safe behavior if a short-circuit is present on the DC-DC output when Vcc of both controllers is generated by the same auxiliary winding.

Figure 22. High-voltage startup, managing the DC-DC output short-circuit

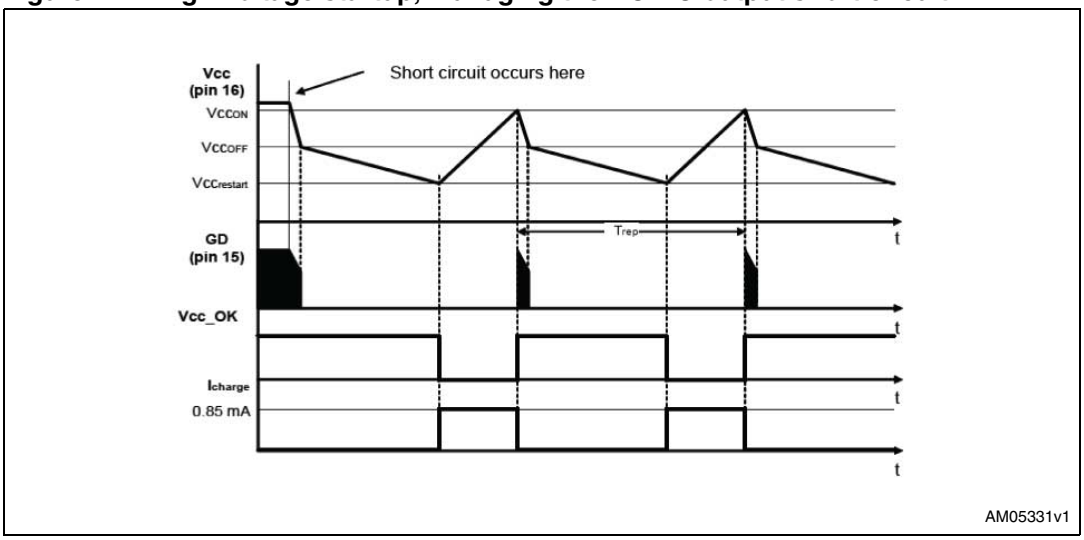


Figure 22 shows how the PFC manages Vcc cycling and the associated power transfer.

At short-circuit the auxiliary circuit is no longer able to sustain Vcc which starts dropping. Reaching its Vcc_{OFF} threshold, the IC stops switching, reduces consumption and drops more until the $Vcc_{restart}$ threshold is tripped. The high-voltage startup generator restarts and when Vcc crosses again its turn-on threshold, the IC starts switching. In this manner the power is transferred from the mains to the PFC output only during a short time for each trip cycle.

5 Design example using the L6563S-TM PFC Excel spreadsheet

An Excel spreadsheet has been developed to allow a quick and easy design of a boost PFC preregulator using the STM L6563S controller or the L6563H version, operating in transition mode. As shown in *Figure 17* and *Figure 18* the package and the pinout are different but most functionalities are the same and therefore they can be calculated in the same way. *Figure 23* and *Figure 24* show the first sheet filled with the input design data used in *Section 3*.

Figure 23. Excel spreadsheet design specification input table

Parameter	Name	Value	Unit [ ]
Mains Voltage Range	VacMin	90	VACrms
Mains Voltage Range	VacMax	265	VACrms
Min.Mains Frequency	fl	47	Hz
Regulated Output Voltage	Vout	400	Vdc
Rated Output Power	Pout	100	W
Max. Output Low Frequency Ripple	ΔVout	20	Vpk-pk
Holdup Capability	Thold	10	ms
Min. Output Voltage after Line drop	VoutMin	300	Vdc
Min. Switching Frequency:	fmin	40	kHz
Expected Efficiency	η	94	%
Expected Power Factor	PF	0.99	---
Maximum Ambient Temperature	Tambx	50	C

AM05336v1

Figure 24. Other design data

Parameter	Name	Value	Unit [ ]
Maximum Magnetic Flux Density	Bx	0.25	T
Ripple Voltage Coefficient	r	0.15	---

AM05337v1

Because in this example the PFC output voltage is required to be stable over the entire input mains range, the TBO function is not used and the TBO pin is left floating on the board. To use the spreadsheet to calculate a PFC circuit with stable output voltage, please set in the specification section $V_{out1} = V_{out2} = V_{outx}$.

The tool is able to generate a complete part list of the PFC schematic represented in *Figure 25* (for L6563S) and *Figure 26* (for L6563H) including the power dissipation calculation of the main components.

Figure 25. TM PFC using the L6563S Excel spreadsheet schematic

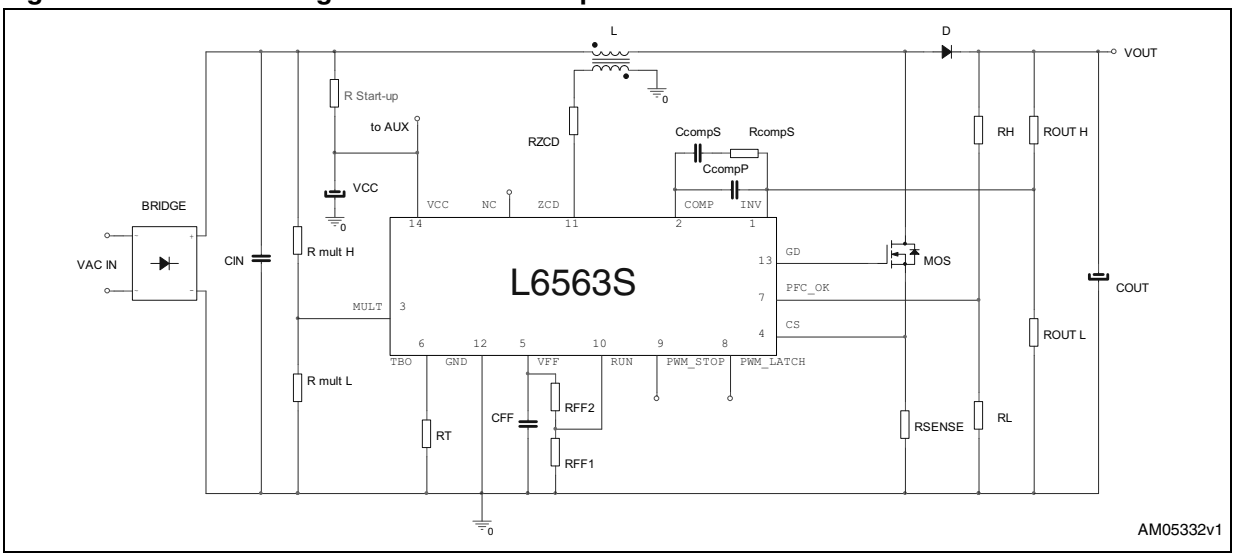
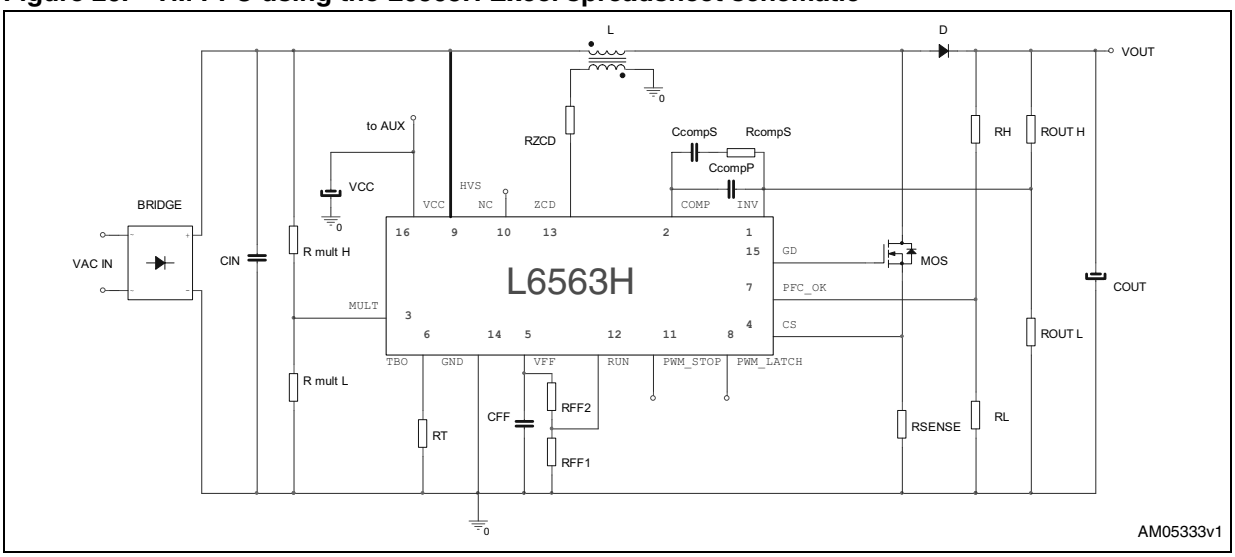
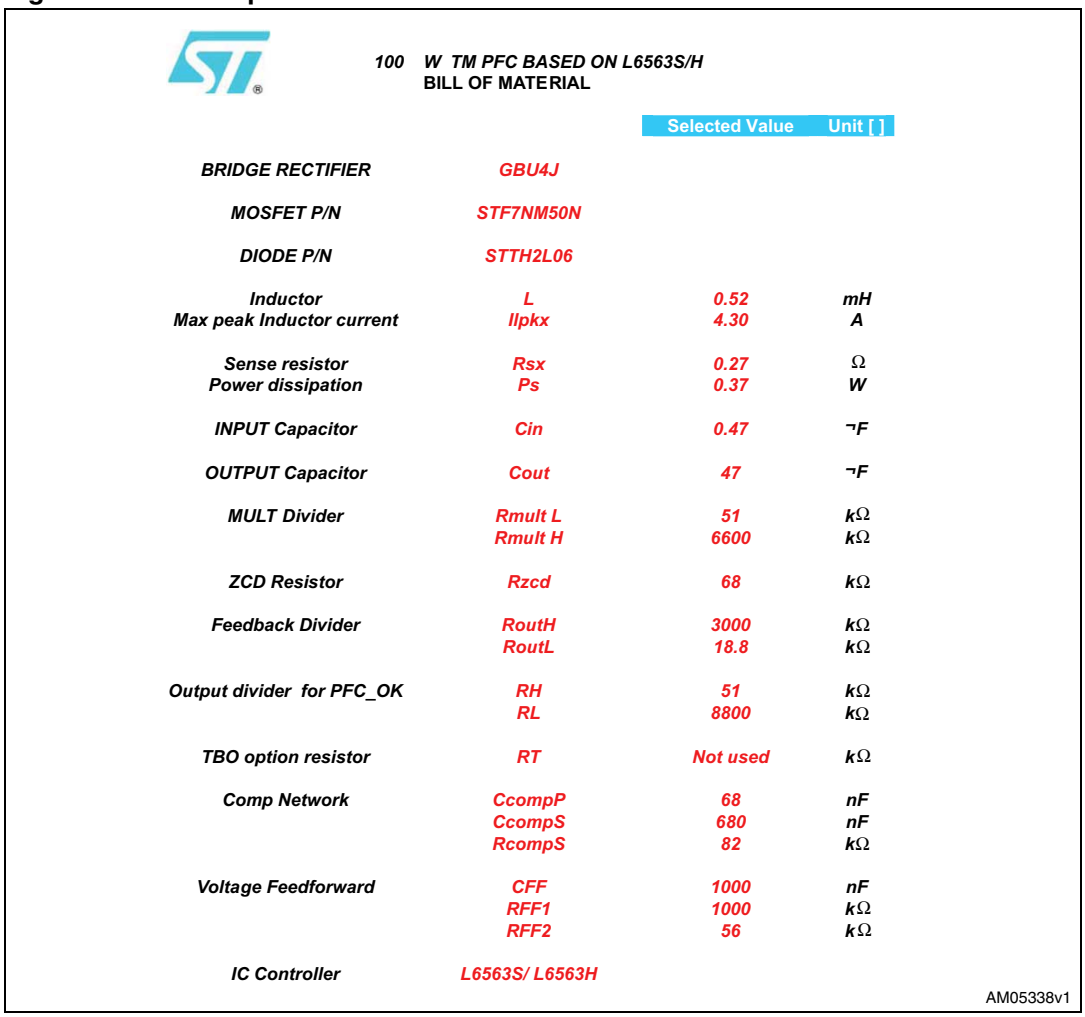


Figure 26. TM PFC using the L6563H Excel spreadsheet schematic



The bill of material in *Figure 27* is automatically compiled by the Excel spreadsheet. It summarizes all selected components and some significant data.

Figure 27. Excel spreadsheet BOM - 100 W TM PFC based on L6563S/H



100 W TM PFC BASED ON L6563S/H
BILL OF MATERIAL

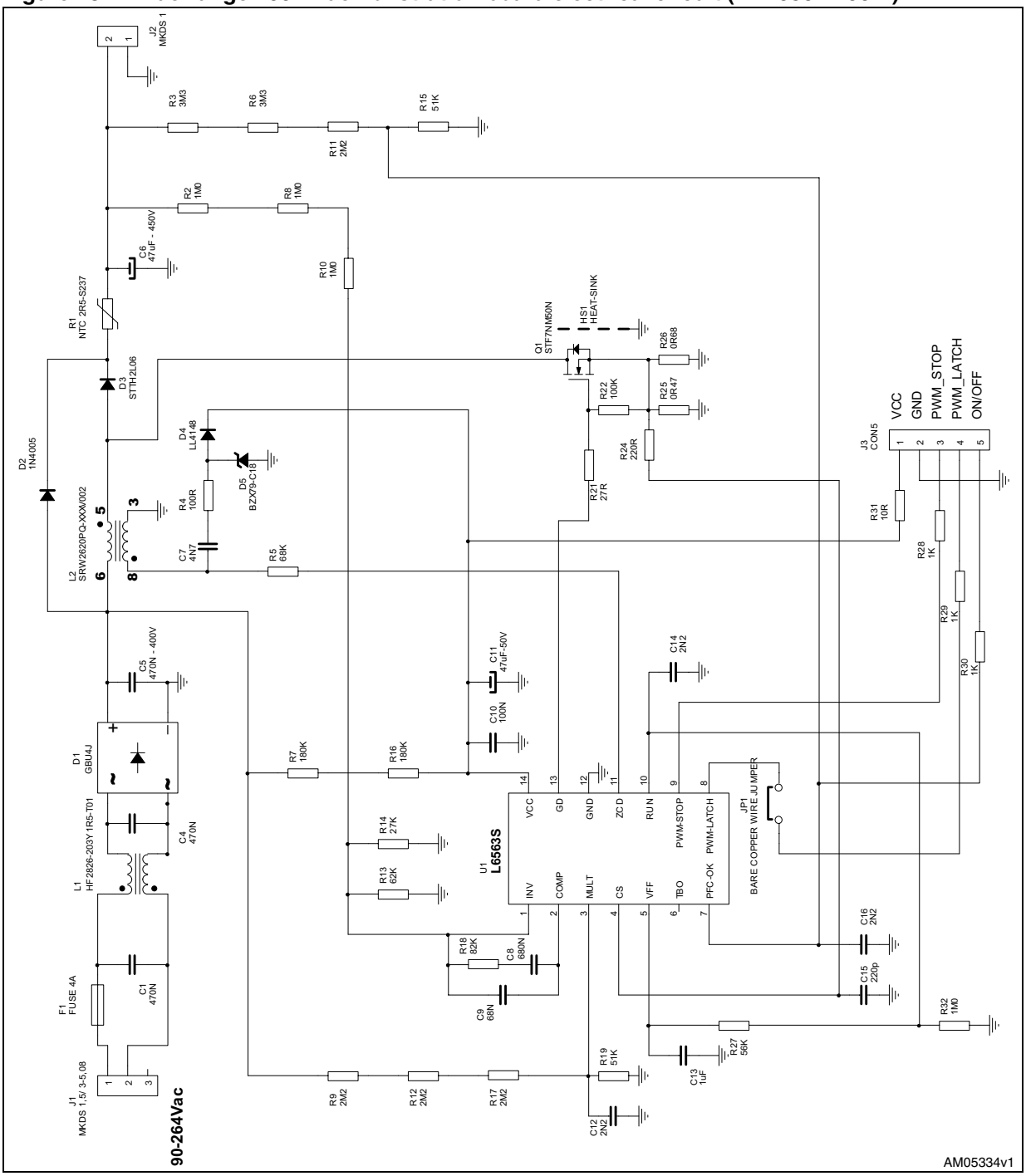
		Selected Value	Unit [ ]
BRIDGE RECTIFIER	GBU4J		
MOSFET P/N	STF7NM50N		
DIODE P/N	STTH2L06		
Inductor	L	0.52	mH
Max peak Inductor current	Ilpkx	4.30	A
Sense resistor	Rsx	0.27	Ω
Power dissipation	Ps	0.37	W
INPUT Capacitor	Cin	0.47	¬F
OUTPUT Capacitor	Cout	47	¬F
MULT Divider	Rmult L	51	kΩ
	Rmult H	6600	kΩ
ZCD Resistor	Rzcd	68	kΩ
Feedback Divider	RoutH	3000	kΩ
	RoutL	18.8	kΩ
Output divider for PFC_OK	RH	51	kΩ
	RL	8800	kΩ
TBO option resistor	RT	Not used	kΩ
Comp Network	CcompP	68	nF
	CcompS	680	nF
	RcompS	82	kΩ
Voltage Feedforward	CFF	1000	nF
	RFF1	1000	kΩ
	RFF2	56	kΩ
IC Controller	L6563S/ L6563H		

AM05338v1

6 EVL6563S-100W and EVL6563H-100W demonstration boards

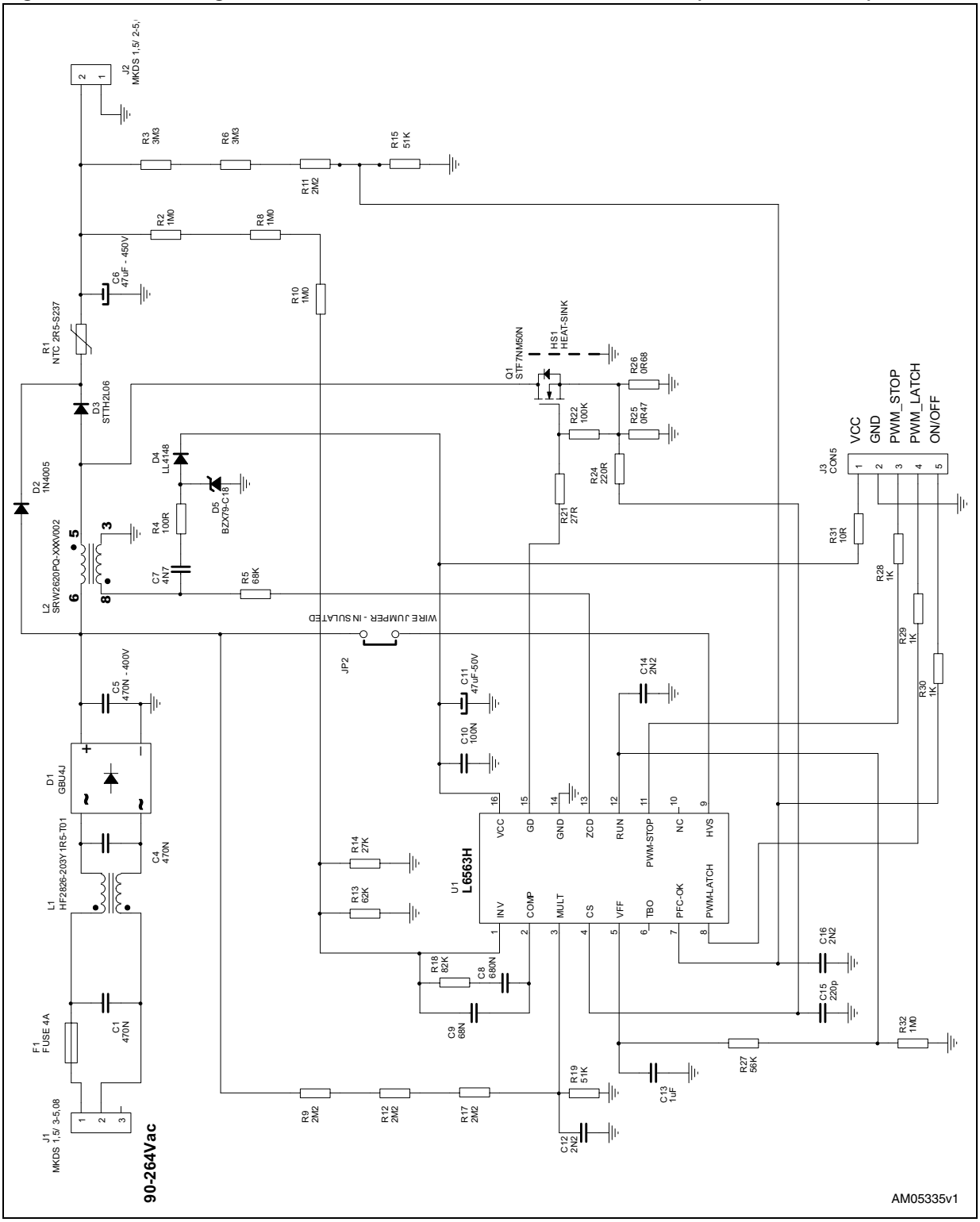
Figure 28 shows the schematic of the 100 W wide-range TM PFC based on the L6563S. It has been dimensioned using the Excel tool presented in *Section 5*.

Figure 28. Wide-range 100 W demonstration board electrical circuit (EVL6564-100W)



Using the same spreadsheet, the schematic of the 100 W wide-range TM PFC based on the L6563H shown in *Figure 29* has been dimensioned too.

Figure 29. Wide-range 100 W demonstration board electrical circuit (EVL6563H-100W)



7 References

1. L6563S datasheet
2. L6563H datasheet
3. “A systematic approach to frequency compensation of the voltage loop in boost PFC preregulator”, abstract
4. AN1089
5. AN3063
6. AN3065

8 Revision history

Table 1. Document revision history

Date	Revision	Changes
28-Apr-2010	1	Initial release.
07-May-2010	2	Modified: *Figure 10* and *24*
22-Oct-2010	3	Modified: *Section 3.4*
09-Feb-2011	4	Updated: *Figure 8*

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